Characterization of Silicon / Silicon Dioxide / LPCVD Silicon Nitride stacks for solar cell application

Hao Jin

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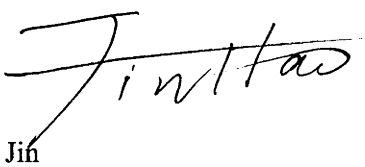
Declaration

I certify that this thesis does not incorporate without acknowledgement any material previously submitted for a degree or diploma in any university, and that, to the best of my knowledge, it does not contain any material previously published or written by another person except where due reference is made in the text. The work in this thesis is my own, except for the contributions made by others as described in the Acknowledgements.



Hao Jin

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Abstract

This thesis is mainly concerned with the surface passivation of crystalline silicon. Continued reductions in the thickness of Si solar cells necessitate improvements to the electronic surface properties, or the degree of surface passivation, of the cells. The degree of surface passivation is influenced by many factors. Obtaining a better understanding of the effects of the various factors, and their interrelationships, requires a combination of various characterisation techniques.

The surface electronic properties are investigated using a set of characterisation techniques which, to the best of the author's knowledge, have not been used in combination before. They are lifetime measurements, Capacitance Voltage (CV) measurements and measurements using the Electron Paramagnetic Resonance (EPR) method. Information about hydrogen in the insulator or at the interface is obtained by Multiple Internal Reflection (MIR) and Secondary Ion Mass Spectroscopy (SIMS) measurements.

Two structures are investigated in the thesis, namely the SiO_2/Si and LPCVD Si_3N_4/SiO_2/Si structures. In both cases, the Si-SiO_2 interface properties are of chief interest. The Si-SiO_2 interface properties are influenced by the oxidation conditions. An in-situ N_2 anneal improves interface properties by reducing the emitter saturation current density J_{oe}. RTA treatments in N_2 are shown to be effective at de-passivating the Si-SiO_2 interface (removal of H_2 without introducing significant additional defects), and can be used in place of vacuum anneals to achieve depassivation. The (111) Si surface is shown to have consistently higher interface recombination velocity than the (100) surface, as well as higher interface defect density D_{it}. The relationship between J_{oe} and D_{it} has also been established.

LPCVD deposited Si_3N_4 films were shown to contain H mainly in the form of N-H bonds, with a relatively small amount of Si-H bonds. High temperature processing (in the range 900-1000°C for 30 mins) results in the removal of the hydrogen by bond breaking. Subsequent high temperature FGA treatments (800-900°C) re-introduce the

hydrogen and result in a re-forming of hydrogen bonds in the nitride film. The temperature for maximum H concentration following a 1 hr FGA was found to be 840°C.

Deposition of LPCVD Si_3N_4 films on SiO_2/Si structures changes the interface properties and introduces additional Si interface defects. LPCVD Si_3N_4 films deposited directly on Si were found to contain a relatively high positive charge density ($\sim 3\times10^{12}$ cm^{-3}) which is reduced somewhat by subsequent thermal treatments. The presence of an intermediate thermal SiO_2 layer resulted in a significant reduction in charge density, with the charge density decreasing with increasing SiO_2 film thickness.

Low temperature atomic hydrogen exposure is a rapid method to introduce hydrogen into LPCVD Si_3N_4 films. A post atomic hydrogen exposure anneal in N_2 is found to further reduce the Si interface recombination velocity.

LIST OF ACRONYMS

ACRONYM	Description
ARC	Antireflection coating
CV	Capacitance Voltage
Cz	Czochralski growth method for crystalline silicon
D_{it}	Density of interface state
EPR	Electron Paramagnetic Resonance
FGA	Forming Gas (5%H_2 in 95% Ar) Anneal
FTIR	Fourier Transform InfraRed
FZ	Float-zone
HFCV	High Frequency Capacitance Voltage
J_{oe}	Emitter saturation current
LPCVD	Low Pressure Chemical Vapor Deposition
MIR	Multiply Inner Reflection
MIS	Metal Insulator Semiconductor
MOS	Metal Oxide Semiconductor
PC1D	Name of one-dimensional numerical semiconductor simulation program for personal computer
PCD	PhotoConductance Decay
Q_f	Fixed charge density
PECVD	Plasma Enhanced Chemical Vapor Deposition
QSCV	Quasi Static Capacitance Voltage
QSSPC	Quasi Steady State Photoconductance
RTA	Rapid Thermal Anneal
SEM	Scanning Electron Microscope
SIMS	Secondary Ion Mass Spectroscopy
SRH	Shockley-Read-Hall
SRV	Surface Recombination Velocity
TCA	$C_2H_3Cl_2$
UV	Ultraviolet
τ_b	Bulk lifetime
τ_{eff}	Effective lifetime

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Introduction

The continued exponential growth of the global photovoltaics market requires a sustained reduction in the cost of PV electricity. At the PV module level, this can be achieved through an increase in module efficiency, or a decrease in module cost, or both. Since the silicon wafer – the starting material for more than 90% of world PV production – constitutes around 50% of the cost of the finished module, a reduction in the wafer cost – achievable through a decrease in wafer thickness – is a requirement. Hence, there is a demand to find methods of producing thinner, more efficient silicon solar cells. As the cell thickness is reduced and the efficiency increases, the surfaces of the solar cell become increasingly important. Thin, high efficiency silicon solar cells require very well passivated surfaces. In contrast, surface passivation in most of the currently available commercial solar cells is comparatively poor, limiting the cell output voltage and conversion efficiency.

In addition to good surface passivation, high efficiency c-Si cells also require good antireflection (AR) control and effective light trapping. The latter requirement arises from the fact that c-Si absorbs infra-red light only weakly. Light trapping is usually achieved by roughening, or texturing, at least one of the surfaces of the active c-Si wafer. The texturing process changes the physical character of the surface and thus influences the fundamental electronic properties. Textured surfaces can display a large range of crystal orientations. In addition, texturing can introduce increased or inhomogeneous interface stress[1] and leads to inhomogeneous dielectric film thicknesses and properties.

A typical surface region is shown in figure 1. It consists of one or more dielectric layers, such as silicon nitride (SiN) or silicon dioxide (SiO_2), a Si-dielectric interface region, and the semiconductor surface, which may be heavily doped. The Si surface is normally textured, which is not shown in the figure. The properties of the interface region – a region around 2-3 nm thick which contains the interface defects - determine to a significant extent the measured electronic properties of the surface, while the properties of all the dielectric layers deposited on the surface,

as well as the properties of the surface texture, determine the optical properties. The optical properties and thicknesses of the dielectric layers thus have to be chosen to ensure that the overall structure acts as an efficient AR coating, once the cell has been encapsulated behind glass in a solar module.

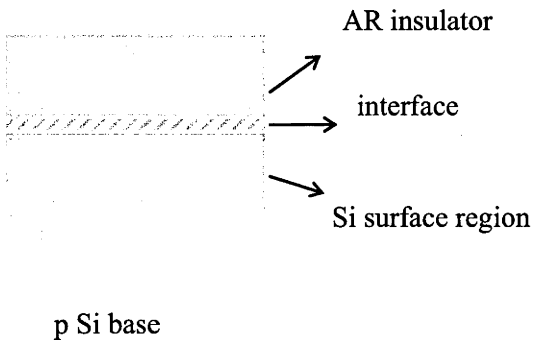

Figure 1. Schematic of the surface structure of a p type solar cell

Silicon dioxide has long been a dielectric of choice for solar cells and other devices due to the ease of growth of a high quality SiO_2 layer by thermal oxidation. Thermally grown SiO_2 provides good surface passivation to p and n type Si substrates, particularly following an anneal in a hydrogen containing atmosphere[2]. In fact, a high quality SiO_2 layer provides the lowest interface defect density achievable with any dielectric material. However, the low refractive index (n=1.46) makes SiO_2 unsuitable as an AR coating following encapsulation. Thick SiO_2 layers (>200 nm) can be used as a diffusion mask, for example, for buried contacted solar cells[3]. However, on textured surfaces the high compressive stress resulting from such a thick oxide can introduce defects into the silicon bulk, resulting in a substantial reduction of the minority carrier lifetime[1].

A key improvement in the last decade has been the introduction of silicon nitride, deposited by plasma enhanced chemical vapour deposition (PECVD). Under optimized deposition conditions, this material allows the achievement of excellent surface passivation, particularly for lightly doped surfaces, and also for heavily doped n type material. The excellent surface passivation stems from both the high density of hydrogen (20-25% depending on the deposition conditions[4, 5] and the positive charges[6] in the PECVD nitride layer. Atomic H is generated during the PECVD nitride deposition process and passivates defects at the Si surface[7], as well as diffusing deep into the Si bulk, where it can passivate bulk defects[8]. The refractive index for the PECVD nitride/Si structure is also nearly ideal (n~2.2) and can be tuned[9]. As a result of these properties, PECVD SiN has become the dominant dielectric for industrial screen printed solar cells. When PECVD SiN is deposited directly on silicon, the critical interface region is usually an oxynitride whose detailed properties and composition depend on the surface preparation and deposition conditions. The interface is inferior to the

Si-SiO_2 interface. PECVD SiN/SiO_2/Si structures have been investigated to a very limited extent, and, as expected, have been shown to display lower surface recombination velocities[10] and better thermal stability[11] than PECVD SiN/Si structures.

There are several limitations with the above technique. One limitation concerns temperature stability. Process temperatures following deposition must in general be kept low to avoid loss of surface passivation. For PECVD SiN films, this is attributed chiefly to a loss of hydrogen from the silicon - silicon nitride interface. Temperatures above 500-600^{0}C usually lead to significant degradation in surface passivation within a period of tens of minutes[12]. Furthermore, high temperature (>800^{0}C) treatments are likely to lead to irreversible degradation of both bulk and surface electronic properties from defects resulting from the high temperature treatment, if the nitride layer is deposited directly on silicon. This limits the use of these films to the end of the cell process. It is not possible, therefore, to deposit the layers early on in the cell process and use them as a process mask layer as well as a passivation / AR coating for the finished cell. A second limitation is that the deposition techniques tend to be directional rather than conformal. This can be an advantage as well as a disadvantage. However, several novel thin film cell approaches, such as the LASE and the Sliver® cell[13] processes rely on conformal deposition techniques for the creation of an AR coating.

A concrete example of the problem of temperature stability is illustrated below. The topside of a solar cell features a layer or a composite of several layers of dielectric material which provide surface passivation and antireflection properties, as well as metal contacts. In a high efficiency cell, the regions under the contacts should be more heavily doped than everywhere else. This structure can be easily realised if the dielectric can be used as the diffusion mask to define the heavily doped regions under the contacts. However, in general this is not possible.

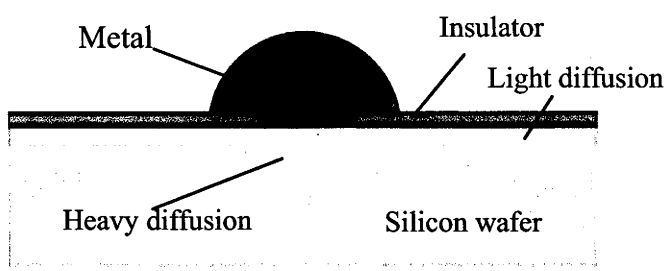

***Figure 2**: Illustration of the features of a typical high efficiency cell in the region of a metal contact. The surface is usually textured; this is not shown.*

An example of a process which utilizes a structure similar to the one shown in figure 2 is the buried contact process[3], used for the fabrication of 'Saturn' cells by BP solar. For this process, the dielectric must also act as a diffusion barrier.

A candidate material for the buried contact process is silicon nitride deposited by low pressure chemical vapor deposition (LPCVD SiN). LPCVD silicon nitride is generally deposited under conditions which result in near stoichiometric films (Si_3N_4). This material has a number of very useful properties. It is extremely hard and scratch resistant; it is resistant to chemical attack in many commonly used etchants for silicon and silicon dioxide (such as hydrofluoric:nitric acid mixtures); it is an excellent diffusion and oxidation mask; it is deposited conformally; and it has a refractive index of 2.0 which makes it well suited as an AR coating. LPCVD silicon nitride can be etched in hot phosphoric acid, which attacks silicon dioxide and silicon only very slowly. All these properties can be exploited in novel cell designs that use the nitride both as a process material as well as an AR coating. Further, LPCVD silicon nitride deposition is a low cost batch process, capable of allowing hundreds of wafers to be processed at a time with good deposition rates typically of the order of 5 nm/sec.

A disadvantage of LPCVD silicon nitride is that it affords little surface passivation. Moreover, similarly to PECVD nitride, the deposition of LPCVD silicon nitride directly on a bare silicon surface can lead to the introduction of defects in the silicon bulk and thus degrade the minority carrier lifetime. This may be attributed to the high levels of intrinsic stress in the as deposited nitride films, typically around 10^{10} dynes/cm^2[14].

Experiments have shown that if a thin, 20 nm layer of silicon dioxide is grown on the surface prior to the deposition of the LPCVD nitride, then excellent surface passivation can be obtained[15]. Such a thin oxide has only a small effect on the AR properties of an optimised oxide / nitride stack. Further, while the surface passivation properties are severely degraded following extended periods of high temperature treatment, this degradation appears to be almost solely the result of loss of hydrogen from the silicon - oxide interface, and it may be possible to recover surface passivation to a significant extent by various means of hydrogen re-introduction.

This thesis explores the properties of silicon dioxide/LPCVD silicon nitride stacks on silicon in detail, in order to obtain a better understanding of such stacks that will ultimately allow the design of improved solar cell fabrication sequences.

Thesis Outline

The thesis is organised into the following parts.

Chapter 1 summarises the main characterisation techniques that were used for the thesis.

Chapter 2 discusses the properties of the Si-SiO_2 interface, and how these are affected by various process parameters.

Chapter 3 explores some of the properties of LPCVD silicon nitride films, and how the deposition of a nitride layer on thermally oxidised silicon influences the Si-SiO_2 interface properties. Further, the introduction of hydrogen to the Si-SiO_2 interface of silicon dioxide/LPCVD silicon nitride stacks on silicon by high temperature forming gas anneals is investigated.

Chapter 4 explores the re-introduction of hydrogen to the Si-SiO_2 interface of silicon dioxide/LPCVD silicon nitride stacks on silicon, using atomic hydrogen.

Suggestions for further work are offered after chapter 4, based on the findings in this thesis.

CHAPTER 1

Measurements of Si surface electrical properties and elemental composition of antireflection coatings

In this chapter, the main characterisation techniques used in this thesis are summarized. The degree of surface passivation is measured by determining the surface recombination velocity. The Si surface recombination velocity is influenced by many factors, such as surface band bending, the interface defect density, the defect distribution within the Si forbidden bandgap and the capture cross sections of these defects. Minority carrier lifetime measurements, using the Quasi Steady State Photoconductance (QSSPC) or transient Photoconductance decay (PCD) methods are used to determine the effective lifetime of Si samples. The emitter saturation current (J_{oe}) can in many cases be determined from these lifetime measurements. Determination of J_{oe}, in turn, allows calculation of the surface recombination velocity (SRV). Lifetime- voltage measurements are also used to determine J_{oe}/SRV and the bulk lifetime. A combination of high

frequency and quasi static capacitance voltage (C-V) measurements is used to determine the defect distribution within the Si forbidden bandgap. Electron paramagnetic resonance (EPR) measurements are used to observe a specific, paramagnetic defect at the Si-SiO_2 interface.

For nitride coated structures, knowledge of the hydrogen content in the nitride layer provides insights into the mechanisms of Si surface passivation and de-passivation with hydrogen. A variant of fourier transform infrared (FTIR) spectroscopy, referred to as the multiple internal reflection (MIR) method, is used to obtain information on H bonds (Si-H and N-H bonds) within the nitride film.

1.1 Measurement of minority carrier lifetime

Recombination is the process whereby electron-hole pairs are lost, with the excess energy released as either photons or phonons. In solar cells, recombination of excess carriers reduces the efficiency of the solar cell. The recombination rate, U, has the following relationship with the recombination lifetime, τ:

$$\tau \equiv \frac{\Delta n}{U} \quad (1.1)$$

where Δn is the excess carrier concentration, $\Delta n = n - n_0$, n_0 is the carrier concentration in thermal equilibrium. This relationship is valid for both electrons and holes.

1.1.1 Recombination mechanics

Bulk recombination

Radiative recombination, band-to-band Auger recombination and recombination via defects are three fundamental Si bulk recombination mechanisms[16]. The bulk lifetime (τ_b), therefore, can be calculated from separate individual lifetimes, as:

$$\frac{1}{\tau_b} = \frac{1}{\tau_{rad}} + \frac{1}{\tau_{aug}} + \frac{1}{\tau_{def}} \quad (1.2)$$

Radiative recombination[16-18] is the inverse process to the absorption of light in a semiconductor. It involves an electron falling down from the conduction band to an unoccupied state in the valance band (a hole). Excess energy is released as the form of a photon. However, the radiative recombination rate in Si is generally considered to be negligible compared with other recombination processes[16], because Si is an indirect-bandgap semiconductor and must

emit a phonon and a photon for both energy and momentum conservation, which involves four particles and is inherently of low probability.

In band-to-band Auger recombination[16-18] an electron recombines with a hole and emits the excess energy to a third charge carrier[19]. Auger recombination will become the dominant recombination mechanism at high injection levels, or in heavy doped silicon.

Radiative recombination and Auger recombination are fundamental properties of the materials and are not influenced by processing.

Recombination via defect sites in the silicon bulk comes from impurities or crystallographic imperfections such as dislocations, which produce discrete energy levels within the Si forbidden bandgap. It is often the dominant recombination process at relatively low injection levels when Si is not heavily doped. The recombination process involves two steps. An electron from the conduction band first relaxes to the defect site and then relaxes to the valence band, where it recombines with a hole[20]. The excess energy is usually released as phonons. The recombination process was analysed in detail by Shockley and Read[21] and Hall[22] (SRH). For a single defect level, the recombination rate, U_{SRH} is given by,

$$U_{SRH} = \frac{np - n_i^2}{\tau_{p0}(n + n_1) + \tau_{n0}(p + p_1)} \quad (1.3)$$

where τ_{po} and τ_{no} are the fundamental hole and electron lifetimes, respectively and n_i is the intrinsic carrier concentration. n_1 and p_1 are statistical factors which depend on the defect's energy level. τ_{po} and τ_{no} are given by

$$\tau_{p0} = \frac{1}{\sigma_p v_{th} N_t} \text{ and } \tau_{n0} = \frac{1}{\sigma_n v_{th} N_t} \quad (1.4)$$

where v_{th} is the thermal velocity, N_t is the defect density, and σ_p and σ_n are the hole and electron capture cross sections, respectively.

Figure 1.1 (taken from reference [17]) shows the lifetime curves for a 1 Ω-cm p type silicon wafer for SRH recombination (with τ_{po}=1 ms and τ_{no}=20 ms), radiative recombination and Auger recombination. SRH recombination normally dominates at low injection levels.

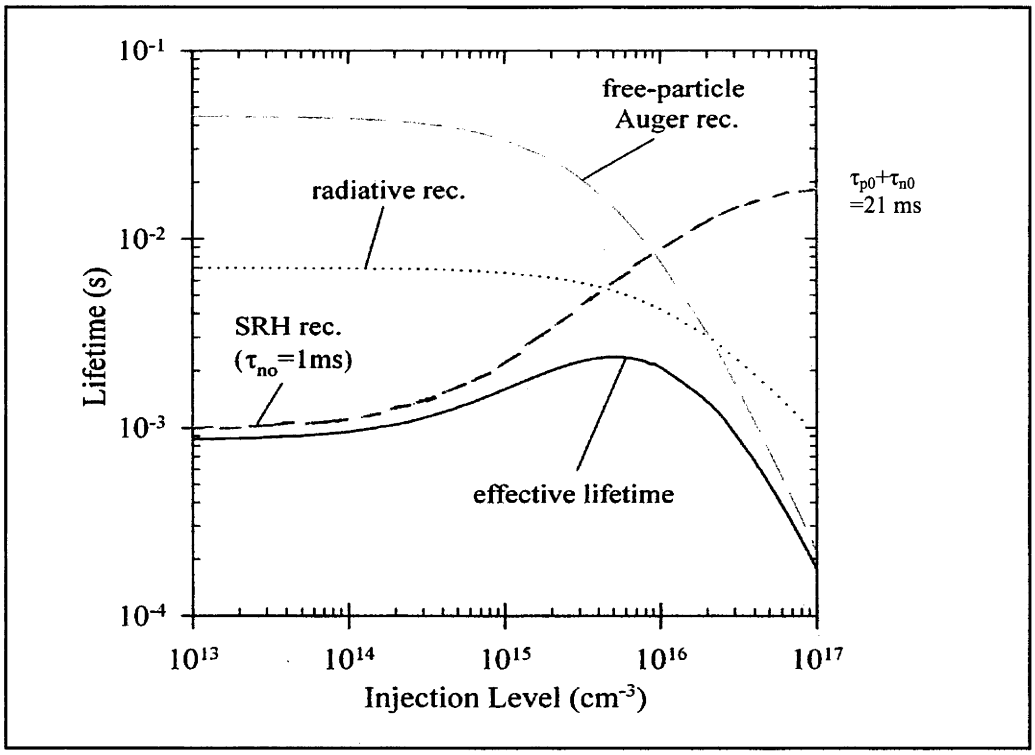

Figure 1.1. Variation of lifetime with injection level for SRH recombination, Auger recombination and radiative recombination.

Surface Recombination

The Si surface or interface defects come from the structural discontinuity of the Si bulk crystal lattice[20]. The defects at the Si surface, in the form of dangling bonds, are distributed continuously within the Si forbidden bandgap. Recombination via defect sites at the Si surface can be modelled by SRH theory. The surface recombination rate U_s via a single-level surface state at energy level E_t is given by:

$$Us = \frac{n_s p_s - n_i^2}{\frac{(n_s + n_1)}{S_{p0}} + \frac{(p_s + p_1)}{S_{n0}}} \quad (1.5)$$

With $S_{no} = \sigma_n v_{th} N_{st}$ and $S_{po} = \sigma_p v_{th} N_{st}$ (1.6)

and $n_1 = n_i \exp(\frac{E_t - E_i}{kT})$, $p_1 = n_i \exp(\frac{E_i - E_t}{kT})$ (1.7)

S_{no} and S_{po} are the surface recombination velocities for electrons and holes, n_s, p_s are the electron and hole concentrations at the Si surface, n_1 and p_1 are statistical factors depending on the defect energy level, E_t, σ_p and σ_n are the cross sections for holes and electrons, and N_{st} is the density of surface states per unit area.

In analogy to equation (1.1), the surface recombination velocity S can be defined as:

$$U_s = S\Delta n_s \quad (1.8)$$

where Δn_s is the excess minority carrier concentration at the surface.

Emitter recombination

In solar cells, the emitter region is usually formed by dopant diffusion. Recombination in the emitter region can be significant compared to recombination elsewhere in the cell. Because the emitter regions are heavily doped, the minority carrier concentration in the emitter region normally remains well below the majority carrier concentration (low level injection) and Auger recombination is likely to be the dominant bulk recombination mechanism. As a result the recombination lifetime in the emitter region is constant with injection level[17], and the recombination current into the emitter, J_{rec}, can be expressed as

$$J_{rec} = J_{oe}\frac{np}{qWn_i^2} \quad (1.9)$$

J_{oe} is the emitter saturation current density; n and p are the electron and hole concentrations on the base side of the space-charge region.

Recombination within the emitter depends strongly on the dopant distribution within the emitter. The emitter saturation current density includes contributions from recombination at the emitter surface as well as the emitter bulk.

The relative contributions of emitter bulk and surface recombination depend on the surface doping concentration and the emitter profile, and in particular its depth. The more heavily doped the emitter (very deep emitter and/or high surface doping), the more insensitive it is to the surface properties. For a phosphorus diffused surface with a sheet resistance lower than 20 Ω/□, the surface has nearly no impact on emitter recombination. When the sheet resistance is lighter than 100 Ω/□, emitter recombination shows a strong dependence on surface passivation. Commercial solar cells usually have sheet resistance ranging from 40-70 Ω/□. However, several cell designs in commercial production or in the research phase have emitters significantly lighter than this.

The emitter recombination lifetime τ_{emit} could be expressed as:

$$\tau_{emit} = \frac{q\, n_i^2 W}{J_{oe}(N_A + \Delta n)} \quad (1.10)$$

where N_A is the dopant density of the Si bulk and Δn is the excess carrier concentration in the Si bulk. When the bulk is in low level injection ($\Delta n << N_A$), the emitter recombination lifetime is independent of injection level. In high level injection, τ_{emit} decreases with increasing injection level, as shown in equation 1.11. This provides the basis for measuring J_{oe}[23, 24].

$$\tau_{emit} = \frac{q\, n_i^2 W}{J_{oe}\Delta n} \quad (1.11)$$

Emitter recombination, as determined by measurement of J_{oe}, includes recombination from the emitter bulk and the surface. If we define the emitter region as the effective surface region, the effective surface recombination velocity, S_{eff}, can be expressed as[25]:

$$S_{eff} = J_{oe}(N_A + \Delta n)/qn_i^2 \quad (1.12)$$

which is also known as the quasi-static emitter approximation.

1.1.2 Effective lifetime

Recombination occurs in the Si bulk and at the surface. The measured lifetime includes the effects of Si surface and bulk recombination and is thus usually known as the effective lifetime, τ_{eff}. In the simplest case, where a sample has a constant bulk lifetime, τ_b, and an effective surface recombination velocity S_{eff} which is low and the same on each surface, the effective lifetime is given by[26]:

$$\frac{1}{\tau_{eff}} = \frac{1}{\tau_b} + \frac{2S_{eff}}{W} \quad (1.13)$$

This relationship is valid if the carrier profiles are relatively uniform throughout the sample bulk. Alternatively, the effective lifetime can be expressed in terms of J_{oe} [23]:

$$\frac{1}{\tau_{eff}} = \frac{1}{\tau_b} + \frac{2J_{oe}(N_A + \Delta n)}{qWn_i^2} \quad (1.14)$$

1.1.3 Lifetime measurement techniques

Various techniques have been developed in order to measure carrier lifetime[27]. This section gives a brief description of the two lifetime measurement techniques used in this thesis, namely the Quasi Steady State photoconductance method (QSSPC) and the photoconductance decay (PCD) method.

1.1.3.1 Quasi Steady State photoconductance method (QSSPC)

Sinton and Cuevas introduced the Quasi Steady State photoconductance method[28]. The experimental apparatus used in this work is shown in figure 1.2.

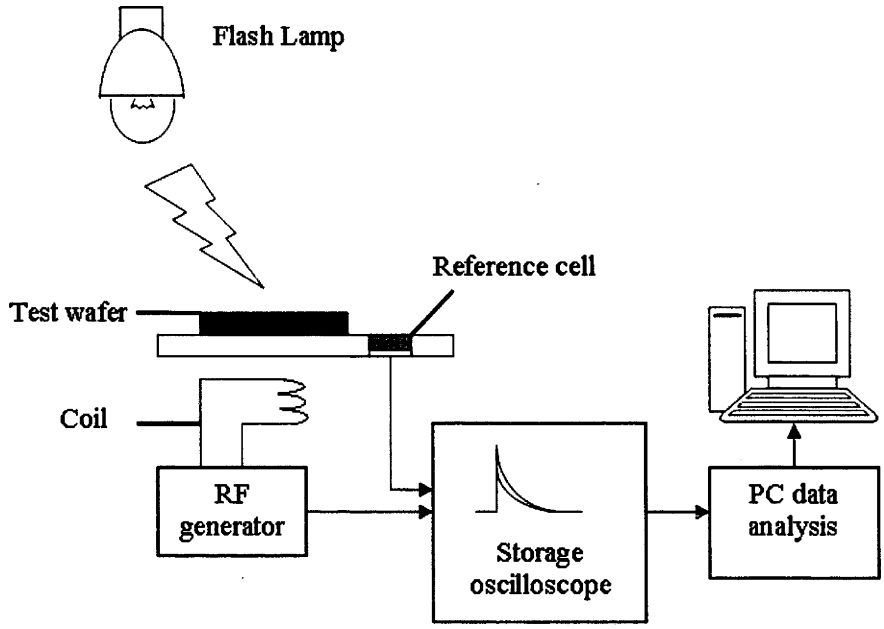

Figure 1.2 Schematic of lifetime measurement apparatus

The experimental sample is inductively coupled by a coil to an rf-bridge circuit. A change in the sample conductivity (as a result of the photogeneration of excess carriers, for example) results in a change in the inductance of the coil, and a change in the output voltage from the circuit. Calibration of the apparatus is achieved by measuring the voltage output for different wafers with a range of known conductance.

In the QSSPC technique the incident light is slowly reduced to zero over several milliseconds. If the effective lifetime of the sample is significantly less than the rate of decay of the light, then the sample can be considered to be in steady state at any one point in time, and the effective lifetime can be determined from a knowledge of the rate of carrier generation and the excess carrier density within the sample. In this way the effective lifetime can be determined over a large range of injection levels. The effective lifetime is calculated using:

$$\tau = \frac{\Delta n_{av}}{g_e} \quad (1.15)$$

where Δn_{av} is the average excess carrier density and g_e is the generation rate produced by incident light. Δn_{av} is calculated by measuring the net excess conductance $\Delta\sigma$:

$$\Delta\sigma = q\Delta n_{av}(\mu_n + \mu_p)W \quad (1.16)$$

g_e is determined by measuring the intensity of the illumination from the flash with a calibrated reference cell, which determines the flux of photons N_{ph}. The test sample will usually only absorb a fraction f_{abs} of the photons absorbed by the reference cell:

$$ge = \frac{N_{ph} f_{abs}}{W} \quad (1.17)$$

f_{abs} must therefore be estimated or experimentally determined for each sample to be measured.

The generalised technique is an extension of the Quasi Steady State photoconductance method, developed by Nagel et al.[29] in which the requirement that the light decay be slow compared to the decay of the excess carriers is relaxed. This is particularly important for samples with a very high effective lifetime (>1 ms). Throughout this thesis, the generalised model of Nagel was used, but the measurement method will be referred to as the QSSPC method.

1.1.3.2 Photoconductance decay (PCD)

In the PCD method, a brief, sharp pulse of illumination is generated and rapidly turned off. Following illumination, the generated carriers decay back to their equilibrium level, which is monitored by the change in photoconductance of the samples. Without significant trapping in Si, the excess carrier concentration is equal for both electrons and holes. The net excess conductance $\Delta\sigma$ is described by equation 1.11. The average excess carrier density Δn_{av} can be calculated for each measured excess conductance $\Delta\sigma$, in conjunction with a carrier density dependent mobility model[30, 31]. The effective lifetime is then calculated via:

$$\tau eff = -\frac{\Delta n_{av}}{d\Delta n_{av}/dt} \qquad (1.18)$$

1.2 Lifetime-Voltage measurements

It is well known that the presence of charge at the Si surface has a significant impact on Si surface recombination, since the presence of such charge changes the surface fermi level (or quasi fermi levels). Strong accumulation or inversion surface conditions (in other words, a high concentration of either electrons or holes at the surface, and therefore a very low concentration of the opposite carrier type in the dark) leads to a low surface recombination velocity. The surface recombination velocity usually reaches a maximum near depletion conditions, when $n_s/p_s=\sigma_p/\sigma_n$ [32].

Various methods are available to vary the charge on the Si surface and investigate in detail its effect on surface recombination. The idea to use an external gate voltage to influence the surface recombination velocity was originally suggested for use in solar cells by Aberle[33]. One method, recently described by Jellett and Weber[34], will be referred to as the

lifetime-voltage method. The method uses a double-sided MOS structure. The Si surface potential is varied by applying a bias voltage and the effective lifetime with the applied voltage bias is measured. Figure 1.7 shows the structure of the samples for lifetime-voltage measurements. Both sides of the samples are coated with a dielectric layer. A very thin layer of Al (~5-8 nm) is thermally evaporated on both sides of the insulator. The dielectric is removed over an area of ~1 cm^2 in order to allow electrical contact to be made to the bulk, realized with Ga/In paste. The sample is then positioned on the coil for lifetime measurement by the PCD method[28].

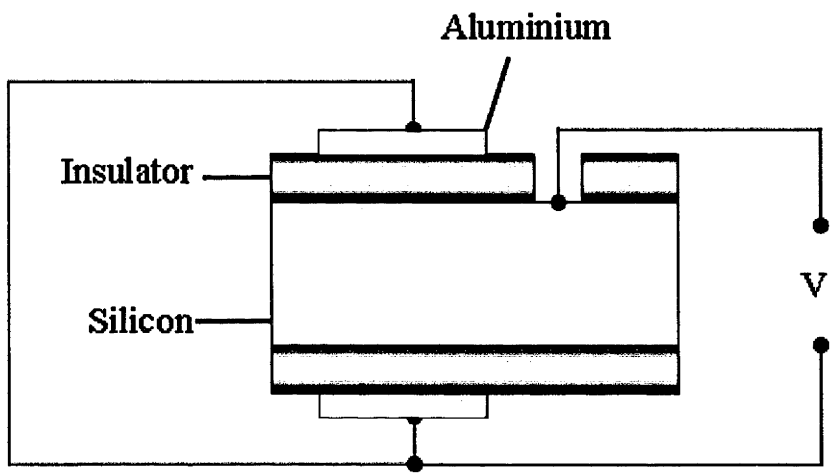

Figure 1.7. Sample structure for lifetime-voltage measurements

Figure 1.8 shows the lifetime-voltage results from a p type (100 ohm-cm) SiO_2/Si structure (undiffused) at an injection level of 4×10^{15} cm^{-2}. The curve displays the typical 'U' shape, with saturation of the effective lifetime under accumulation and strong inversion conditions.

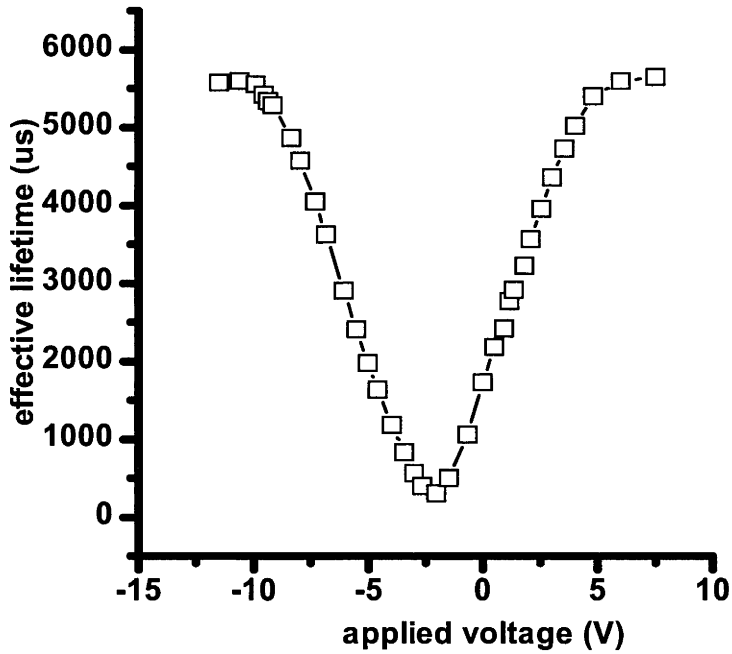

Figure 1.8 A typical lifetime-voltage curve(p type high resistivity FZ Si sample with 50 nm thermal grown oxide on both sides. FGA was carried out before Al deposition.)

1.2.1 Measurement of emitter saturation current

Under accumulation or inversion conditions, holes or electrons will gather in the Si bulk just underneath the surface, forming an ultrathin, heavily doped region. Two conditions for accurate measurement of J_{oe} are that

i) the bulk is in high level injection and

ii) the surface is in low level injection.

Provided the surface concentration of electrons or holes is sufficiently high (~10^{18} cm^{-3} or greater) both these conditions can be met, and J_{oe} can be extracted from the lifetime measurements. Figure 1.9 shows the J_{oe} values for the same p type SiO_2/Si structure as for figure 1.8. The 'dip' in the J_{oe} values for voltages in the range -3V to 0V is due to the fact that, in this voltage range, condition ii) above is not met, ie the surface is not in low level injection during measurement, since the concentration of electrons/holes in the dark is below 10^{18}cm-3. The J_{oe} values in this voltage range are therefore not meaningful.

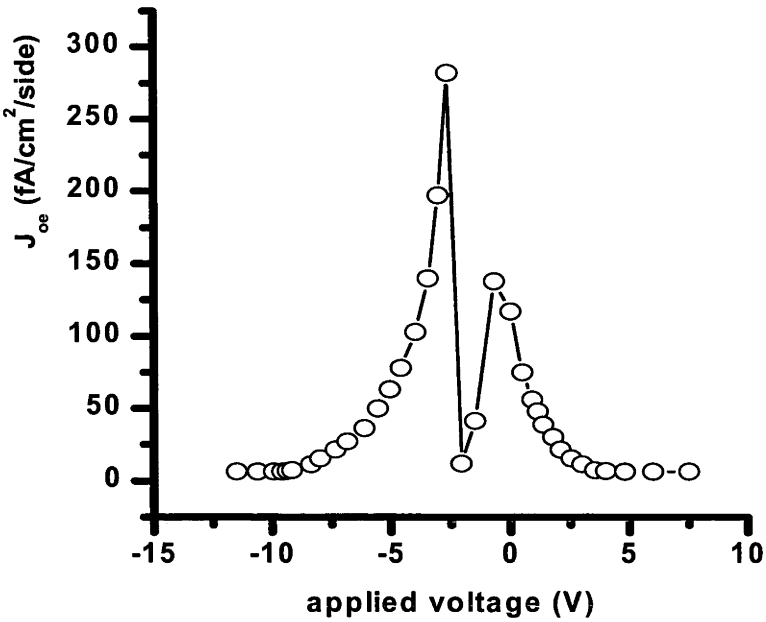

Figure 1.9. applied bias dependent J_{oe}

1.2.2 Determination of recombination velocity and bulk lifetime

The Si bulk lifetime can be determined by analysing the results from the lifetime-voltage measurements. Knowledge of J_{oe} and the effective lifetime (both measured at the same injection level) allows determination of the bulk, high level injection lifetime τ_{hli}. (from equation 1.14). In principle, any pair of J_{oe}-τ_{eff} values, for which the J_{oe} measurement is valid, can be used and should give the same extracted value of τ_{hli}. In practice, τ_{hli} would be expected to be most accurate when J_{oe} is as low as possible. The value of τ_{hli} for the sample used in figures 1.8 and 1.9 is calculated to be around 9.6 ms.

Once τ_{hli} is known, S_{eff} can be calculated using either equation 1.13 (valid for all applied bias voltages, provided that the excess carrier density remains relatively constant throughout the bulk) or using the relationship between S_{eff} and J_{oe} (compare equations 1.13 and 1.14). The latter also allows calculation of S_{eff} at an injection level other that the injection level used for the measurement.

1.3 Measurement of Si interface properties by the Capacitance-Voltage method

For decades the Metal-Insulator-Semiconductor (MIS) structure has been one of the most useful structures for studying semiconductor surface properties. An in-depth description of this method is given by Nicollian[35] and Sze[36].

1.3.1 Metal Insulator Semiconductor (MIS) structure

As shown in figure 1.3, one side of the semiconductor material is covered by an insulator while the other side has an ohmic contact. Metal dots are normally deposited on the insulator. A variable voltage is then applied across the structure and the capacitance is measured.

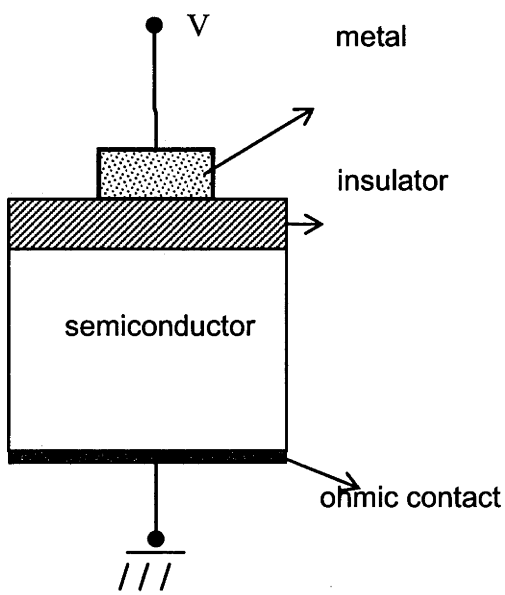

Figure 1.3 Metal Insulator Semiconductor structure

For an ideal MIS structure[36], no charge exists in the insulator layer and the work function difference between semiconductor and metal is zero:

$$\Phi_m - (\chi + \frac{Eg}{2q} - \psi_B) = 0 \qquad (1.19) \text{ for n type and}$$

$$\Phi_m - (\chi + \frac{Eg}{2q} + \psi_B) = 0 \quad (1.20) \text{ for p type}$$

where Φ_m is the metal work function, χ is the semiconductor electron affinity, E_g is the Si bandgap, ψ_B is the potential difference between the Fermi level E_F and the intrinsic Fermi level E_i.

For an ideal MIS structure, no band bending occurs when no bias is applied. When a voltage is applied across the MIS structure, band bending occurs at the surface. Figure 1.4 shows the energy band diagram for a MIS structure on p type Si for different applied voltages.

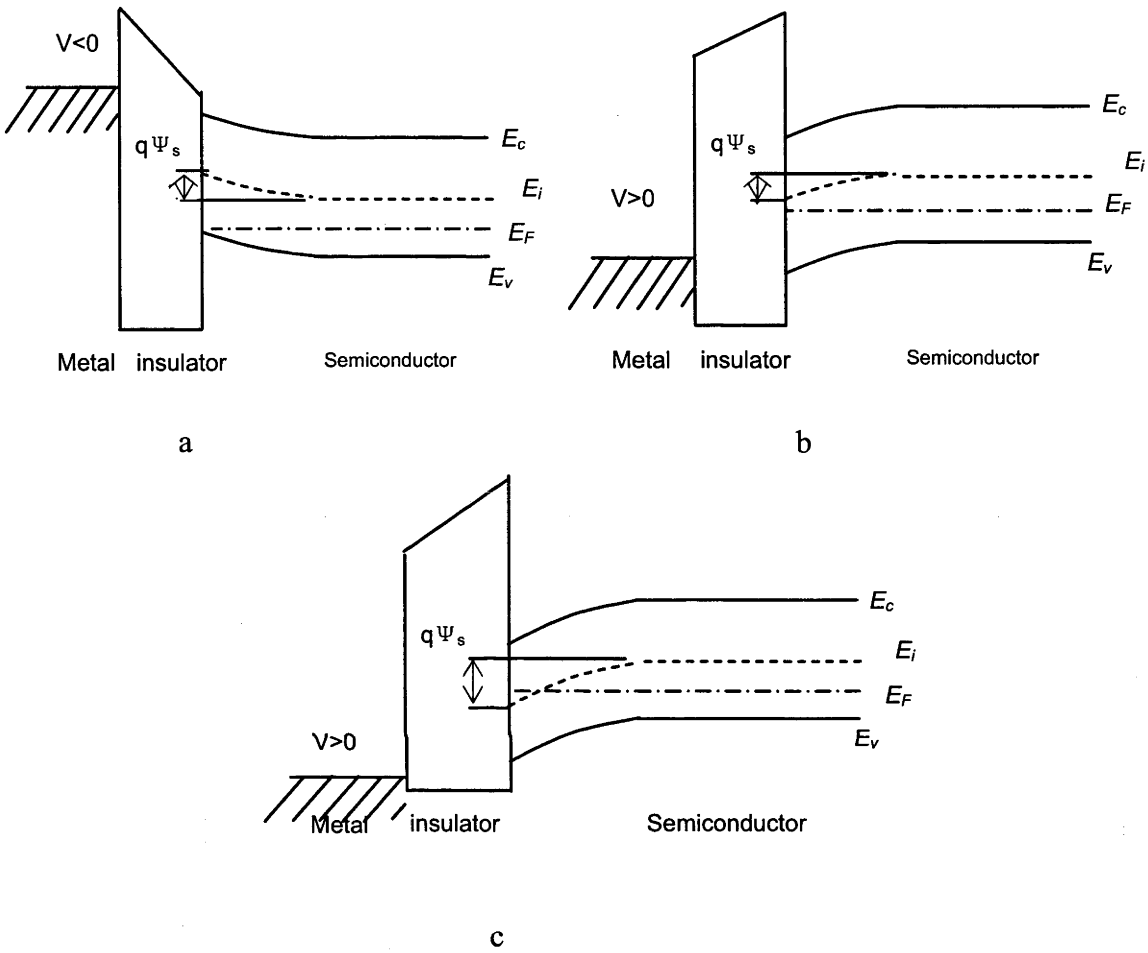

Figure 1.4 Energy band diagram for ideal p type Si for case of (a) accumulation (b) depletion (c) inversion at the surface

- When a negative voltage is applied, holes accumulate at the Si surface and the bands bend upwards, resulting in a Si surface potential $q\Psi s < 0$, as shown in figure 1.4(a). Flat band conditions exist when no voltage is applied $q\Psi s = 0$.

- When a positive voltage is applied, holes are depleted from the Si surface region and the bands bend downwards with $q\Psi s > 0$, shown in figure 1.4(b).

- With an increase of the applied positive voltage, strong band bending occurs and the intrinsic Fermi level falls below the Fermi level at Si surface. The majority carriers in the

surface region are electrons in this case and the surface is therefore in inversion, figure 1.4(c). Strong inversion occurs when $q\Psi s > 2(E_F-E_{i,})$, where E_i refers to the intrinsic Fermi level in the Si bulk.

1.3.2 Calculation of charge density in the insulator and interface defect density

By varying the dc gate voltage, the MIS structure is driven from strong inversion to accumulation. A small ac voltage with adjustable frequency is superimposed on the dc gate voltage and the differential capacitance of the MIS structure is measured.

Kuhn[37] found that low-frequency C-V properties of semiconductor diodes can be measured by observing displacement currents with the application of a linear ramp voltage to the diode when the ramp rate β (=-dV/dt) is selected to be low (β ~0.01 V/s). The capacitance C of the sample is given as

$C=I_d/\beta$ (1.21)

where I_d is the observed displacement current. He called this technique a quasi-static C- V method. He applied this method to crystalline silicon metal-oxide-semiconductor (MOS) diodes to characterize the Si/SiO_2 interface states.

When the Si surface is in accumulation, the majority carriers are attracted to the Si surface. The semiconductor's capacitance is very large and the total capacitance is close to the insulator capacitance. When the majority carriers are depleted from the Si surface, the semiconductor's capacitance is reduced, resulting in a decrease of the total capacitance. In the accumulation region, the frequency of the ac voltage has no influence on the measured capacitance.

When the fermi level at the Si surface passes the intrinsic fermi level (strong depletion, $\Psi s = \Psi_b$) and further moves to inversion, the total capacitance reduces to a minimum and then increases as an inversion layer of electrons (for p type Si) or holes (for n type Si) forms at the surface. This only happens at a sufficiently low frequency when the generation-recombination rate of minority carries can keep up with the ac-signal variation leading to a charge exchange with the inversion layer in step with the measurement signal[36]. If the frequency is high, the minority carrier charge exchange due to generation and recombination is too slow to keep with the ac signal. As a result, the high frequency capacitance remains low in the inversion region.

Calculation of charge density

For an ideal MIS structure with no bias applied, the energy band at the surfaces are flat. However, in a real structure charges exist in the insulator layer and at the semiconductor-insulator interface. The voltage at which the energy band is flat is defined as the flat band voltage, V_{fb}. It has the following relationship with the charge in the insulator:

$$V_{fb} = -\frac{Q_f + Q_m + Q_t}{C_i} \qquad (1.22)$$

where Q_f is the fixed interface charge, Q_m is the effective net charge of mobile ions per unit area at the Si-insulator interface, and Q_t is the effective net trapped charge in bulk insulator traps per unit area at the Si-insulator interface. They are given by,

$$\frac{Q_m}{C_i} = \frac{1}{C_i}[\frac{1}{d}\int_0^d x\rho_m(x)dx] \quad \text{and} \quad \frac{Q_t}{C_i} = \frac{1}{C_i}[\frac{1}{d}\int_0^d x\rho_t(x)dx] \qquad (1.23)$$

where d is the insulator thickness, and ρ_m and ρ_t are the volume charge densities of the mobile ions and trapped charges, respectively.

Normally charges in SiO_2 and SiN_x layers on Si are positive, resulting in downward band bending. Therefore, a negative voltage needs to be applied to achieve flat band conditions.

Taking into account a nonzero metal-semiconductor work function difference ϕ_{ms}, equation (1.15) can be written as:

$$V_{fb} = \phi_{ms} - -\frac{Q_f + Q_m + Q_t}{C_i} \qquad (1.24)$$

If mobile and trapped charges in the insulator can be neglected, the equation can be simplified to:

$$V_{fb} = \phi_{ms} - \frac{Q_f}{C_i} \qquad (1.25)$$

Capacitance voltage (CV) measurements are made by first sweeping from inversion to accumulation. If the sweep is from accumulation to inversion, the sweep rate has to be slow enough to avoid the deep inversion effect[38] for high frequency C-V curves. Sweeping from inversion to accumulation results in a 'proper' high frequency C-V curve independent of sweep rate[38]. CV curves at high frequency and under quasi static conditions for SiO_2/Si structures are shown in figure 1.5. A (100), p type, 10-23 Ωcm, Si wafer was used for the curve in figure 1.5 (a) and a (100), n type, 3-10 Ωcm, Si wafer was used for the curve in figure 1.5 (b). A 100 nm thick oxide layer was thermally grown on Si followed by an in-situ anneal in N_2 at the oxidation temperature and an anneal in forming gas (FGA) at 400°C for 30 minutes.

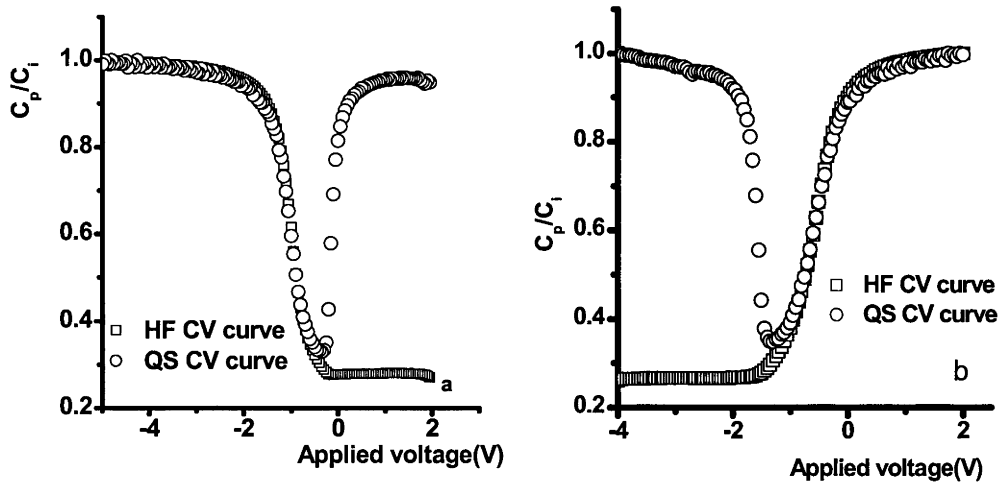

Figure 1.5. High frequency and Quasi Static CV curves for (a) p type and (b) n type Si/SiO_2 structures.

From these curves, important information like insulator thickness, Si substrate doping, flat band voltage, surface potential and interface defect distribution within the Si forbidden bandgap, can be extracted.

Determination of insulator thickness

In the accumulation region, the measured capacitance C_p is close to the insulator capacitance, C_i, since the high density of accumulated holes for p type Si and electrons for n type Si results in a high differential semiconductor capacitance[36]. The insulator thickness d is calculated via:

$$C_i = \frac{\varepsilon_i}{d} \qquad (1.26)$$

where ε_i is the dielectric constant for the insulator.

Determination of Si doping level

In the strong inversion region, the measured capacitance C_{min} from the high frequency CV curve has the following relationship with the maximum depletion width, W_m,:

$$C_{\min} = \frac{\varepsilon_i}{d + \frac{\varepsilon_i}{\varepsilon_s} W_m} \qquad (1.27)$$

where ε_s is the dielectric constant for the semiconductor

W_m has the following relationship with doping level, N_A:

$$W_m = (4\varepsilon_s kT\ln(\frac{N_A}{n_i})/(q^2 N_A))^{\frac{1}{2}} \qquad (1.28)$$

Where K is Boltzmann's constant and q is the electronic charge. Therefore, the doping level can be calculated from C_{min}.

Determination of flat band voltage

The flat band voltage is determined from the high frequency CV curve. As shown in figure 1.4 (a), the series combined capacitance C is:

$$C = \frac{C_i C_D}{(C_i + C_D)} \qquad (1.29)$$

At flat band conditions, the depletion layer capacitance is given by:

$$C_D = \frac{\varepsilon_s}{L_D} \qquad (1.30)$$

where L_D is the Debye length and is given by:

$$L_D = \sqrt{\frac{\varepsilon_s kT}{q^2 N_A}} \qquad (1.31)$$

The flat band capacitance can be calculated from a combination of equations 1.29, 1.30 and 1.31.

Determination of interface defect density and surface potential

Various techniques, e.g. Terman[39], Kuhn[37], Castagne[40] have been developed to determine the interface defect density D_{it}. Terman and Kuhn's methods depends on a single frequency measurement at high frequency and low frequency, respectively. These methods determine D_{it} with relatively low accuracy. By comparing the MIS capacitance at high and low frequency, Castagne pointed out the areal interface defect density, D_{it}, has the following relationship with capacitance:

$$D_{it}(V_g) = \frac{1}{qA}\left(\frac{C_i C_{QS}}{C_i - C_{QS}} - \frac{C_i C_{HF}}{C_i - C_{HF}}\right) \qquad (1.32)$$

where A is the surface area, C_{QS} is the quasi steady state capacitance and C_{HF} is the high frequency capacitance. The surface potential Ψs is determined by Berglund's formula[41]:

$$\psi_s(V_g) = \int_{V_{fb}}^{V_g}\left(1 - \frac{C_{QS}(V_g)}{C_i}\right)dV_g \qquad (1.33)$$

Combining equations 1.22 to 1.33, a computer program was written in Matlab to analyse the D_{it} distribution within the Si forbidden bandgap. p type Si samples can be used to obtain information about the upper half of the bandgap and n type Si samples for the lower half of the bandgap. Figure 1.6 shows the D_{it} distribution derived from the curves shown in figure 1.5

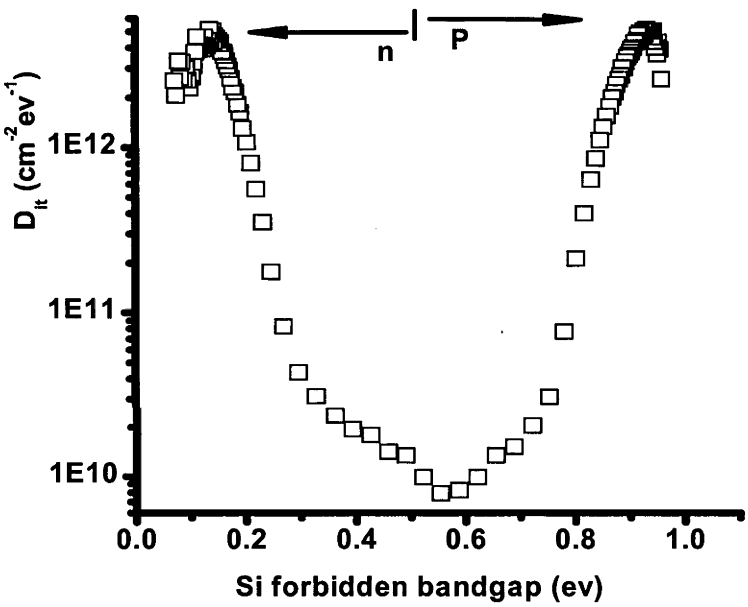

Figure 1.6. D_{it} in the Si forbidden bandgap for an SiO_2/Si structure

1.4 Measurement of paramagnetic interface defects by Electron Paramagnetic Resonance

Electron Paramagnetic Resonance (EPR), also called Electronic Spin Resonance (ESR), is the tool which can identify specific defects at the Si surface and insulator bulk from insulator coated Si structures. In 1970, Yoshio Nishi[42] first detected three paramagnetic signals from the (111) Si-SiO_2 interface by EPR and labeled them as P_a, P_b, P_c, respectively. He ascribed the P_b centers to an unpaired electron on a threefold coordinated silicon atom at or very near the interface. He

also examined their behavior after different treatments. Later, P_a was demonstrated to be from donor or conduction electrons[43] whereas P_c was due to contamination[44]. Caplan[45] et al. presented evidence that confirmed the P_b structure as an unpaired electron in a sp^3-hybridized dangling bond orbital at the Si interface, as shown in figure 1.10(a). Brower's observation of ^{29}Si hyperfine provided conclusive evidence of the defect structure[46]. Brower also pointed out that the P_b signal's shape (linewidth) and position (g value) varies with direction of the applied magnetic field[47]. EPR studies also determined that this P_b defect is the most important source of interface states in as-processed[45, 48, 49], irradiated[50, 51], field stressed[52, 53], and hot carrier stressed[54, 55] (111) Si-SiO_2 interfaces. The reaction of hydrogen with P_b centers was also identified by EPR measurements[56-61]

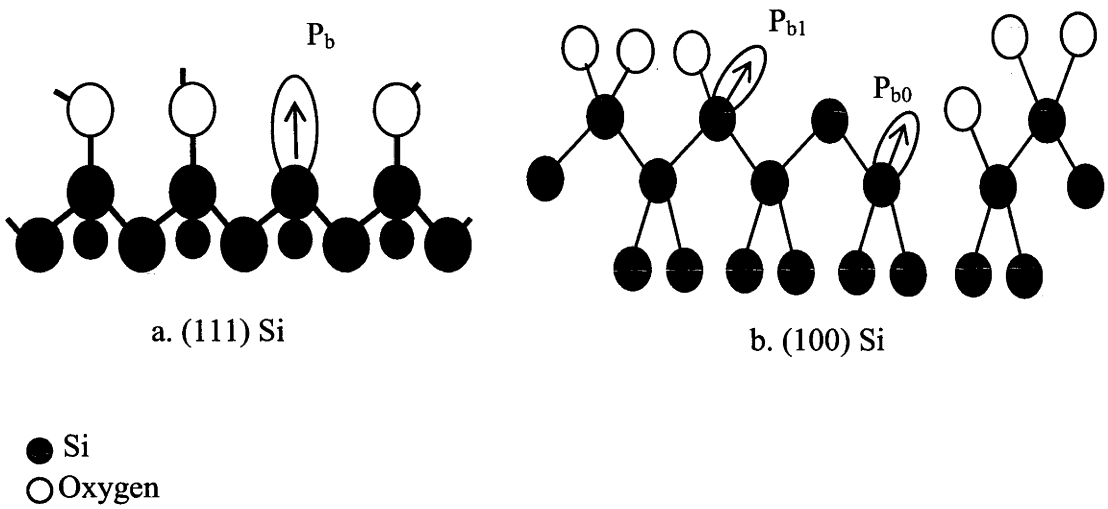

Figure 1.10. Paramagnetic defects at (a) (111) Si surface. (b) (100) Si surface.

Most of the EPR work has been done with (111) oriented Si surface. Poindexter[48] identified two centres at the (100) Si-SiO_2 interface, called P_{b0} and P_{b1}. As shown in figure 1.10 (b), P_{b0} is thought to be chemically the same as P_b at the (111) Si surface with the structure $\cdot Si{\equiv}Si_3$, whereas P_{b1} is believed to have a geometry similar to P_{b0}, but chemically and paramagnetically different, with the structure $\cdot Si{\equiv}Si_2O$. However, there is still some controversy about the exact nature of P_{b0} and P_{b1} [62-64]. The band-gap energy distribution of P_b centers was determined for both (111) and (100) Si surface[63, 65]. The origin of the paramagnetic defects was generally believed to stem from accumulated stress from the oxide layer on the Si-SiO_2 interface; however, Futako[66], by in-situ EPR measurements during ultrathin SiO_2 growth on (111) Si, pointed out that the P_b properties and density are little influenced by oxide thickness, and that therefore the P_b defect density does not originate from the long-range accumulation of the structural stress between two materials, but from the reaction of oxidation within a few Si atomic layers.

Stesmans and his co-workers made significant contributions to understanding the P_b signal from the Si-SiO_2 interface. He determined the dependence of the P_b signal on the

frequency band used[67], as well as its dependence on oxidation conditions[68]. He observed the influence of post oxidation thermal processes[69-72], the influence of annealing in molecular hydrogen[73-79], and the influence of in-situ applied stress during oxidation[80] on the properties and concentration of P_b centers. He also found a new intrinsic defect in the as grown SiO_2 layer, called the EX centre[81-83].

1.4.1 Mechanics of Electronic Paramagnetic Resonance

Paramagnetic entities exist in a great number of materials. The capability of EPR measurement results from the magnetic moment of an unpaired electron's spin, which is very sensitive to local magnetic fields within the sample. These fields often originate from various nuclei's nuclear magnetic moments, which could be present within the bulk and surface of the medium.

Applying a strong magnetic field B to paramagnetic species containing material, the individual magnetic moment arising via the unpaired electron "spin" can be oriented either parallel or anti-parallel to the applied magnetic field. This creates distinct energy levels for the unpaired electrons, making it possible for net absorption of electromagnetic radiation (in the form of microwaves) to occur. Magnetic resonance takes place when the magnetic field 'matches' the microwave frequency, which means the microwaves energy corresponds to the energy difference, DE, of the pair of involved spin states, as:

$$DE = \hbar\nu = g\beta B \qquad (1.34)$$

where h is Planck constant, υ is the microwave frequency, g is the Zeeman splitting factor and β is the Bohr magneton.

1.4.2 EPR operation and signal calibration

EPR measurements of the Si interface defect (P_b) centers were undertaken using a Bruker 300E spectrometer operating at X Band (9.44GHz), fitted with an Oxford ES-9 liquid helium cryostat with temperature control via an Oxford ITC-4 controller. Measurements were done using a modulation frequency of 100KHz, modulation amplitude (M_A) of 5G and a microwave power of 20μW at a temperature of around 8.5K. The low temperature is realized by immersing the tubes containing the samples into liquid helium. The defect spin at the Si interface saturates when a high microwave power is applied. 20μW was observed to be non-saturating. Samples were placed in 3 mm ID quartz EPR tubes, which were flushed with pure argon to remove oxygen. The sample tubes were sealed with rubber septa and the sample end frozen to 77K. The angle between the sample surface and the magnetic field is less than 3°.

The spectrum shown in figure 1.11 was obtained at a temperature of around 8.5K, MA of 10.145 G and microwave power of 0.5 mW. A $CuSO_4$ solution of known molarity is used for

instrument calibration. The conditions used for obtaining the Cu^{2+} spin signal are similar to those used for measuring P_b centers in order to allow a direct and accurate comparison between the two signals.

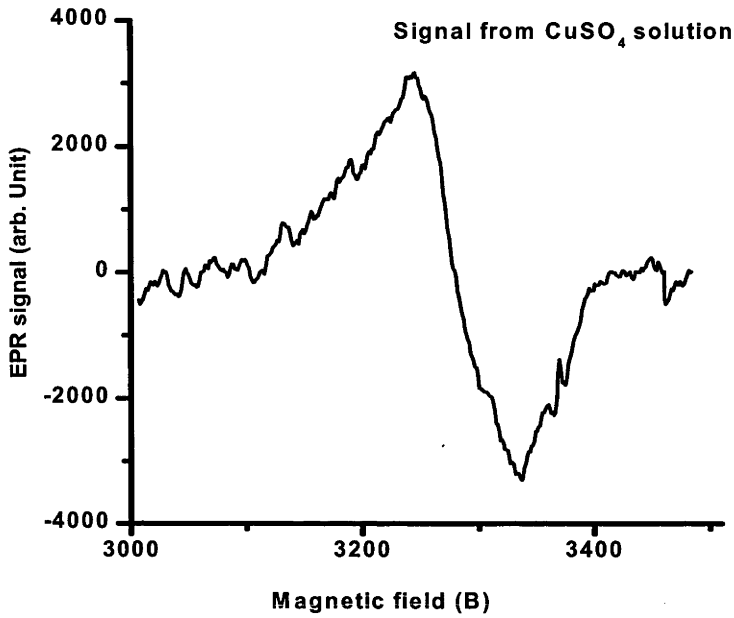

Figure 1.11. EPR spectrum from $CuSO_4$ solution

The total spin number is calculated from the following equation:

$$Spin = K\frac{DI \times (\frac{SW_G}{\#\,pts})^2 \times T(K)}{M_A \times G_N \times \sqrt{MWP(W)}} \qquad (1.35)$$

where K is a constant determined by calibration with the $CuSO_4$ solution, DI is the absolute value of the signal obtained by double integrating the spin signal, SWG is the swept field width, #pts is the resolution, G_N is the receiver gain level, MWP(W) is the microwave power in the unit of watt, and T(K) is the temperature in Kelvin.

From the solution signal, K is determined to be 2.24×10^{11}. All spin density calculations in this work are obtained with this K value.

Si substrates used for EPR measurement were p-type, ~10 Ω-cm, (111) Cz wafers. Samples were cut with a diamond saw into 25 mm×2.5 mm pieces to fit in the EPR cavity. They were subsequently etched in 15:1 HNO3:HF solution for 3 minutes to remove saw damage from the surfaces. A standard RCA clean and DI water rinse were carried out before EPR measurement. At low microwave power, the EPR signal is very sensitive to experimental conditions. The tube containing the samples should be free from contamination and crystal defects. Etching of the silicon samples is necessary for removing the Si edge signals from the cutting process. The presence of phosphorus can also lead to an additional signal which overlaps with the P_b signal. Figure 1.12 shows the EPR signals from a tube (curve a, with crystal defects from a tiny crack),

from an un-etched Si edge (curve b, with g=2.006) and a small amount of phosphorus from a P diffusion (curve b, doublets with distance of around 42G). These signals can interfere with the P_b signal (g value from around 2.00-2.01) and should be eliminated.

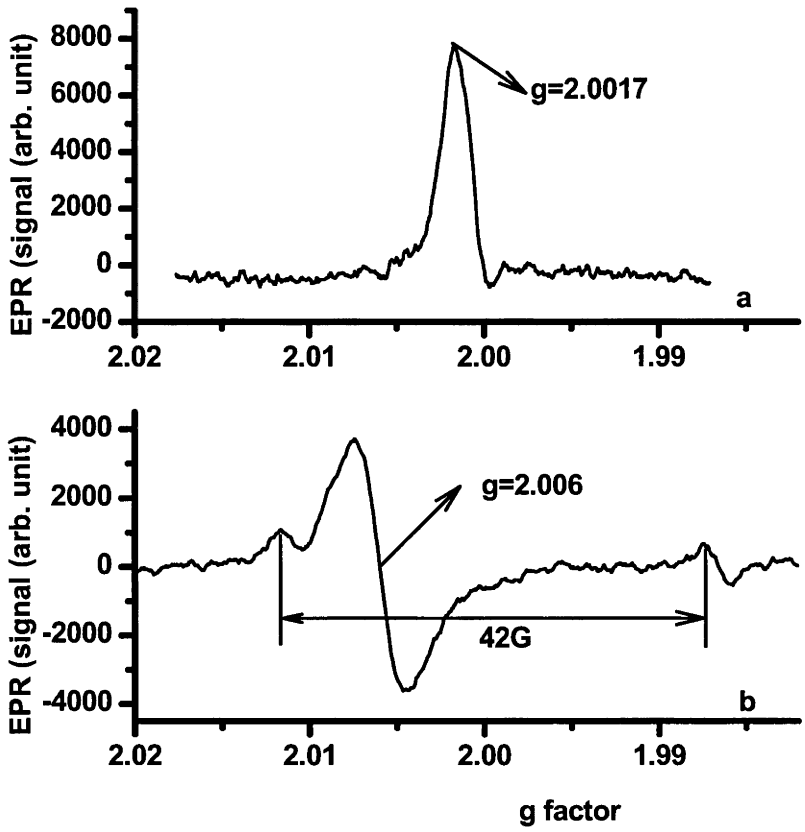

Figure 1.12. EPR spectrum from (a) tube with tiny crack and (b)sample with small amount of phosphorus (doublets) and Si edge signal from cutting process (centre signal)

1.5 Measurement of bonded hydrogen concentration by Multiple Internal Reflection

The bonded hydrogen concentration in thin films can be investigated by Fourier Transform Infrared spectroscopy (FTIR). Details of the operation of FTIR measurements can be found in other publications[84].

The principle for FTIR can be simply described as follows. Chemical bonds vibrate at specific frequencies. The resonant frequencies can be related to the strength of the bond, and the mass of the atoms at either end of it. Thus, the frequency of the vibrations can be associated with a particular bond type. When the frequency of incident radiation coincides with its natural vibrational frequency, a transition from one vibration state to another in the electronic ground state occurs, which is accompanied with a change in the linear dipole moment. The vibration

may be infrared-active, and an absorption band associated with the transition will be seen in the infrared spectrum. For FTIR measurements, the light is not separated into its individual frequencies. Instead, all frequencies are incident on the sample at the same time, and the sample response to all frequencies is detected simultaneously.

FTIR has been widely applied in determining H bond concentrations, configurations and their influence on the properties of nitride films. FTIR is well suited, for example, for the study of H in Plasma Enhanced Chemical Vapor Deposited (PECVD) silicon nitride films[85-91] due to the relatively high H concentration in these films. However, FTIR is not sensitive enough to accurately measure the much smaller concentrations of bonded H in LPCVD nitride films of typical thickness (in the order of 50 nm). In this case, other techniques, such as nuclear analysis or elastic recoil detection can be used instead to determine the areal H concentration and even the concentration profile[4, 92-94]. However, these techniques were not readily available and do not give information on the H bond state.

1.5.1 Principle of Multiple Internal Reflection

For thin films with low bonded H concentrations, such as LPCVD Si_3N_4 films on Si, the technique of Multiple Internal Reflection (MIR) can be used to enhance the sensitivity of FTIR measurements[95-98]. An in depth description of MIR is given by Harrick[99]. A brief summary is presented here.

When light, traveling in a medium with refractive index n_1, in incident upon an interface with another medium with refractive index $n_2 < n_1$, total internal reflection will occur if the following criterion is satisfied:

$$\theta \geq \sin^{-1}\left(\frac{n_2}{n_1}\right) \quad (1.36)$$

where θ is the angle of incidence of the light. In this case, an evanescent wave is set up in the less dense medium whose intensity decays exponentially with distance into the medium. The penetration depth d_p, is defined as the distance required for the electric field amplitude to fall to e^{-1} of its value at the interface, and is given by:

$$d_p = \frac{\lambda}{2\pi n_1 (\sin^2\theta - n_{21}^2)^{1/2}} \quad (1.37)$$

where λ is wavelength of the light in free space and $n_{21}=n_2/n_1$.

The application of MIR to the study of LPCVD Si_3N_4 films with low H concentration is illustrated in figure 1.13. Light is coupled into one of the edges of the sample, which have been ground and polished to make an angle of 45° with the sample surface. The light is made to be incident perpendicular to the sample edge, so that it travels though the sample at an angle of 45° with respect to the (polished) surfaces. Given the refractive indices of Si and Si_3N_4 (3.42 and

2.05 respectively), the criterion for total internal reflection is satisfied, and the light remains trapped within the structure, undergoing multiple internal reflections, before exiting on the other side. At each reflection, the light penetrates through the Si_3N_4 film and absorption occurs at the characteristic frequencies corresponding to Si-H and N-H bonds. In this way, it is possible to increase the strength of the absorption signal by increasing the number of internal reflections.

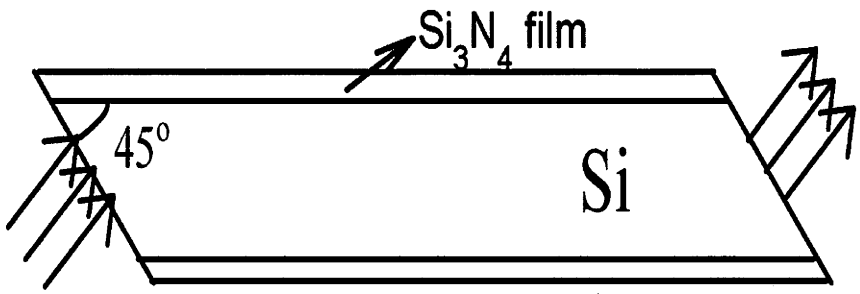

Figure 1.13. The structure of the samples for MIR measurements.

For MIR measurements, typically 200 nm thick LPCVD Si_3N_4 films were deposited on 500 μm thick double sided polished Si wafers. A bare Si sample was used as a reference sample for extracting the background signal. The wafers were cut into 8 mm×10 mm×0.5 mm pieces. Light enters the samples perpendicularly to the edge surface and reflects about 20 times at the Si-Si_3N_4 interface before exiting. The penetration depths for IR light into the nitride film are 349 nm for N-H bonds and 535 nm for Si-H bonds, respectively. The N-H (at the wavelength of 3326 cm^{-1}) and Si-H (at the wavelength of 2210 cm^{-1}) absorption peaks from an as deposited LPCVD Si_3N_4 film after baseline correction and smoothing are shown in figure 1.14.

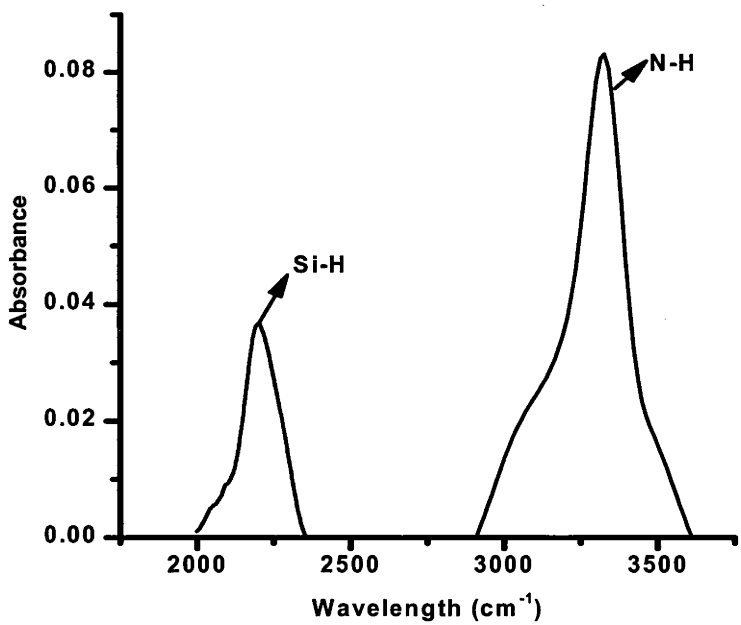

Figure 1.14 MIR spectrum of the N-H bonds (at 3326 cm^{-1}) and Si-H bonds (at 2210 cm^{-1}) from 200 nm LPCVD nitride on both side of double sides polished Si samples.

1.5.2 MIR Calibration

The calibration of the H bond FTIR spectrum is discussed in detail by Lanford and Rand[100]. By integrating the N-H and Si-H spectra and comparing with the results from the nuclear analysis method, they concluded that Si-H bonds in nitride film have about 1.4 times the specific absorption of N-H bonds. Total hydrogen concentration per unit area [H], can be written as:

$$[H] = [Si-H] + [N-H] = 1.36 \times 10^{17} \times (1.4S_{N-H} + S_{Si-H}) \quad (1.38)$$

where [Si-H] and [N-H] refer to Si-H bond and N-H bond area concentrations, respectively, and S_{N-H} and S_{Si-H} refer to the area of the Si-H and N-H bond spectra, respectively.

The H atom concentration, $[H]_a$, has the relationship with [H] as:

$$[H]_a = \frac{[H]}{L\rho_{SiN}} = \frac{[H]\cos\theta}{2n_r L_0 \rho_{SiN}} \quad (1.39)$$

where L is the effective film thickness, n_r is the reflection time, L_0 is the nitride film thickness and ρ_{SiN} is the atomic density of the nitride film.

It should be noted that the absolute accuracy of the MIR technique as used here is estimated to be no better than +/-20%. Errors are introduced by several factors, such as the requirement to know accurately the values of film thickness, refractive index at the relevant wavelength, and film density; deviation in the angle of the light relative to the sample surfaces from 45°; and the fact that the signal obtained is relatively noisy and requires baseline correction and smoothing.

1.6 Summary

This chapter briefly described the main characterisation techniques used in this thesis. Lifetime and lifetime-voltage measurements, Capacitance-Voltage measurements and Electronic Paramagnetic Resonance measurements are combined to analyse different aspects relating to the Si-SiO_2 interface. Lifetime and lifetime-voltage measurements allow determination of the (effective) surface recombination velocity and in many cases, the emitter saturation current density. These are the parameters of practical interest for solar cells as they have a direct bearing on the magnitude of the short circuit current, open circuit voltage and fill factor losses of a solar cell.

C-V measurements allow determination of the effective interface charge density and the defect density distribution within the Si forbidden bandgap. Both parameters directly affect the effective Si surface recombination velocity.

Only one specific type of defect, the paramagnetic interface defects, can be observed by Electronic Paramagnetic Resonance measurements. The defect density is determined by double integration of the defect signal and comparing with a standard solution signal obtained at the similar conditions.

Multiple Internal Reflection (MIR) measurements can be used to obtain information on Si-H and N-H bond densities in insulator layers. MIR enhances the sensitivity of the standard FTIR technique, an important feature for LPCVD Si_3N_4 layers which have a relatively low H concentration. Table 1.1 summarises the main techniques.

	Insulator (SiO_2, SiN_x)	Si surface	
		Undiffused	Diffused
QSSPC	×	τ_{eff} and S	τ_{eff} and J_{oe}
Lifetime-Voltage	×	S, J_{oe}, τ_{eff} and τ_b	S, J_{oe}, τ_{eff} and τ_b
CV	Thickness, charge density	D_{it}	×
EPR	Bulk paramagnetic defect density	P_b	×
MIR	Si-H and N-H bonds	×	×

Table 1.1. Summary of main characterisation techniques used in the thesis work

The use of different substrates and insulator thicknesses throughout the thesis work was dictated by the requirements of the characterisation techniques. For C-V measurements, moderately doped wafers are required for accurate results, while the unambiguous extraction of the emitter saturation current density J_{oe} requires the use of lightly doped material as well as diffused surfaces (except for the lifetime-voltage technique, where Joe can also be extracted for undiffused surfaces), since extraction of J_{oe} requires measurement with the wafer bulk in high level injection, but the surfaces in low level injection. It is therefore unfortunately not possible to carry out the various measurements on identical samples. Similarly, the choice of oxide thickness was dictated by the characterisation technique to some extent. For example, 100 nm has been found to be the optimal oxide thickness to obtain the most accurate results from C-V measurements. While the use of different substrates and oxide thickness makes a quantitative comparison impossible, qualitatively the various surfaces display the same trends with the various treatments.

CHAPTER 2

Si-SiO_2 interface properties of SiO_2/Si structures

Silicon dioxide has been widely used and investigated as an effective passivation and antireflection layer for Si solar cells. In this chapter, the electrical properties of the Si-SiO_2 interface of SiO_2/Si structure are discussed. The Si-SiO_2 interface properties show a strong dependence on oxidation conditions, Si surface conditions and post oxidation thermal treatments. Dry and wet (with trichloroethane) oxidations at different temperatures are compared. The surface recombination velocity of (100), (111) and textured Si surfaces is

studied. Si surfaces between planar (100) and inverted pyramid textured surface were realized by acid etching. Post oxidation thermal treatments, such as in-situ nitrogen anneals, hydrogenation and dehydrogenation are applied and their influence on the Si surface recombination velocity is studied. The influence of the phosphorus diffusion on Si surface passivation is discussed.

2.1 Introduction

For decades, silicon dioxide has been widely used for the passivation of Si surfaces in the microelectronic and photovoltaic fields. Owing to its importance, the Si-SiO_2 system has become the most intensively investigated semiconductor-insulator system. A well prepared SiO_2 layer provides good Si surface passivation due to a low interface defect density.

Thermal oxidation of Si wafers is realized in a clean quartz tube at 800-1200°C. Pure oxygen or water vapor flow (wet oxidation) travels from one end of the tube to the other side, diffusing through the oxide layer and reacting with the Si substrate to form silicon dioxide

$Si+O_2$ --- SiO_2 (2.1)

for dry oxygen and

$Si+2H_2O$ --- SiO_2+2H_2 (2.2)

for water vapor. The final oxide layer is approximately 54% above the original surface of the silicon and 46% below the original surface. The oxide thickness is proportional to reaction time in the early stage of oxidation, when growth rate is limited by the reaction at the silicon interface. For longer oxidation time, the oxide thickness is proportional to the square root of time, as the oxidation rate becomes diffusion limited.

The oxide growth rate depends mainly on reaction temperature, pressure, time, oxidant composition and Si surface orientation. The reaction occurs more rapidly at higher temperatures. Water vapor has a much higher diffusivity than oxygen in silicon dioxide, which accounts for the higher oxide growth rate in a wet atmosphere. Hence, the addition of a few percent of trichloroethane (TCA) into the oxygen flow will enhance the oxidation reaction rate since water vapor is created during the burning of TCA. The oxygen diffusion rate through oxide is proportional to the partial pressure of the oxidizing species, so growth shows a strong dependence on pressure. The oxidation rate also depends strongly on Si surface orientation. The crystal orientation changes the number of silicon bonds available at the silicon surface, which influences the oxide growth rate. Under certain reaction conditions, the (111) Si surface has a 20-30% higher oxidation rate than the (100) Si surface.

In this chapter, the electrical properties of the Si-SiO_2 interface are examined by lifetime, lifetime-voltage, CV and EPR measurements. Factors affecting the interface defects, e.g., oxidation conditions, insitu annealing, thermal annealing and phosphorus diffusions, are

discussed. The Si-SiO_2 interface thermal stability is also investigated. (111) and (100) oriented Si surface properties are compared.

2.2 Fundamental properties of the as grown, hydrogenated and dehydrogenated Si-SiO_2 interface

A thermally grown oxide is stoichiometric. However, a ~2-3 nm layer of non-stoichiometric oxide exists just above the Si substrate[36]. The interface defects (dangling bonds) exist in this region. The interface is mainly characterized by Q_f, Q_{it} and D_{it} [35, 36].

- Q_f is the density of fixed positive charges believed to exist very close to the Si-SiO_2 interface. The Q_f defects are characterized by a Si atom bonding with three oxide back bonds and one dangling bond. In contrast to the interface charge Q_{it} described below, Q_f is independent of Fermi level position at the Si surface. Q_f is constant and can not be altered by the surface band bending caused by illumination or gate bias.

- Q_{it} is the trapped charge density associated with interface states within the Si forbidden bandgap and is strongly dependent on Fermi level. The trapped charges can be donor-like or acceptor-like or amphoteric interface states. At a well-prepared Si-SiO2 interface, Q_{it} is much smaller than Q_f.

- D_{it} is the density of interface states within Si forbidden bandgap, resulting from the discontinuity of the crystal lattice. The interface states cover the whole Si forbidden bandgap. The interface states contribute to surface recombination.

Hydrogen plays a critical role in Si surface passivation. Interface defects (dangling bonds) can be passivated (made electrically inactive) by bonding with hydrogen, which can be realized by annealing in a hydrogen containing atmosphere, as shown in equation 2.3, where D represents the defect. Conversely, hydrogenated defects can become electrically active by losing H, as shown in equation 2.4, which can be realized by annealing in a hydrogen free atmosphere at elevated temperatures.

$$2D+H_2 \longleftrightarrow 2DH \qquad (2.3)$$

$$2DH \longleftrightarrow 2D+H_2 \qquad (2.4)$$

D_{it} within the Si forbidden bandgap can be dramatically reduced by means of bonding dangling bonds with hydrogen, since the energy levels of hydrogen terminated dangling bonds are beyond the Si forbidden bandgap. Hydrogenation of the Si-SiO_2 interface is usually realized by annealing in forming gas (FGA) at temperatures between 350 to 450°C. Conversely, dehydrogenation of the Si-SiO_2 interface can result from thermal treatments in a hydrogen free atmosphere and leads to an increase of the electrically active interface defect density. Deliberate de-hydrogenation can be achieved by vacuum annealing [71, 72] or rapid thermal anneals (RTAs) [101].

Stesmans pointed out that annealing in vacuum at high temperature can break the P_b-H bonds and activate the P_b signal. However, vacuum annealing above 640°C also results in SiO bond rupture and the generation of additional P_b centres[71, 72]. Vacuum annealing at 800°C for about 1 hour generates about 4×10^{12} /cm^2 extra P_b centres[71, 72].

Hurley[101] showed that an RTA in N_2 at high temperature (≥800°C) could be used as an alternative to vacuum annealing to activate the interface P_b centres. In this thesis, RTAs in N_2 at 800°C were performed in most cases to activate the P_b signal. Since we do not have free access to vacuum annealing, the comparison between RTA and vacuum annealing is only discussed briefly in Table 2.9. We choose a relatively low annealing temperature to minimize the generation of additional defects.

2.2.1 Experimental details

For CV measurements, p/B, (100), 10-23 Ωcm, Cz, ~500 μm thick wafers and n/P, (111), 3-10 Ωcm, Cz, ~500 μm wafers were used. It is assumed that the difference in doping concentration will not influence the Si interface properties, like the D_{it} values. Treatments applied to the CV samples are listed in table 2.1. Samples for QSSPC measurements are p type, (100), FZ, >100 Ωcm, 550 μm wafers and n type, (111), FZ, ~100 Ωcm, 550 μm wafers. Treatments applied to these samples are listed in table 2.2 Samples for EPR measurements are p type, (111), Cz, ~10 Ωcm, 500 μm wafers. Treatments to the EPR samples are listed in table 2.3.

All furnaces received a TCA clean at 1100°C for at least 30 minutes prior to loading of the samples. Figure 2.1 shows the Scanning Electron Microscope (SEM) picture of patterned and textured Si surface. Textured regions occupy 67% of the Si surface region.

Step	Description	Chemical	Details
1	Saw damage etch	HF:HNO_3 solution	Remove saw damage from Si surface and edges by etching in HF:HNO_3 solution for 3 minutes.
2	HF dip	10% HF solution	Until hydrophobic to remove native

			oxide
3	Cleaving	--	Wafers were cleaved into quarters and labeled.
4	RCA clean 1	5:1:1 H_2O:NH_4OH:H_2O_2 solution	For 10 minutes in warm solution (~80°C)
5	RCA clean 2	5:1:1 H_2O:HCl:H_2O_2 solution	For 10 minutes in warm solution (~80°C)
6	HF dip	Clean 10% HF solution	Until hydrophobic to remove native oxide
7	Oxidation	Oxygen with or without TCA	In TCA cleaned tube at high temperature to grow ~100 nm oxide layers, followed by an insitu anneal in N_2 at the oxidation temperature for 30 minutes.
8	Forming gas anneal (FGA)	Forming gas (5% H_2 in 95% Ar)	Selected samples receive FGA at 400°C for 30 minutes to hydrogenate the Si-SiO_2 interface
9	One side oxide removal	HF fuming	One side of oxide was removed by HF fuming
10	Al deposition	Al	At high vacuum ($<3\times10^{-6}$ torr), ~80 nm thick Al was thermally evaporated (all through the thesis) on oxide layer through a shadow mask with area of 4.7×10^{-3} cm^2
11	Ohmic contact	Ga-In	Ohmic contact by Ga-In paste on oxide free Si side.

Table 2.1 Experimental processes for CV sample preparation

Step	Description	Chemical	Details
1	Quartering	---	For (111) samples, wafers were cut by a diamond saw into quarters and labelled
2	Saw damage etch	HF:HNO_3 solution (1:10)	Remove saw damage from Si surface and edges by etching in HF:HNO_3 solution for 3 minutes.
3	HF dip	10% HF solution	Until hydrophobic to remove native oxide
4	Texturing	TMAH	Some (100) samples were patterned and textured to form inverted pyramids, the SEM picture of the textured surface is shown in figure 2.1.
5	Cleaving	--	(100) wafers were cleaved into quarters and labelled.
6	RCA clean 1	5:1:1 H_2O:NH_4OH:H_2O_2 solution	For 10 minutes in warm solution (~80°C)
7	RCA clean 2	5:1:1 H_2O:HCl:H_2O_2 solution	For 10 minutes in warm solution (~80°C)
8	HF dip	Clean 10% HF solution	Until hydrophobic to remove native oxide
9	Oxidation	Oxygen	In TCA cleaned tube at 1000°C to grow ~50 nm oxide layers, followed by an insitu anneal in N_2 at the oxidation temperature for 30 minutes on selected samples.

10	Forming gas anneal (FGA)	Forming gas (5% H_2 in 95% Ar)	All samples receive FGA at 400°C for 30 minutes to hydrogenate the Si-SiO_2 interface
11	Rapid thermal anneal (RTA)	N_2	RTA at 500°C or 600°C for 3 minutes to dehydrogenate the Si-SiO_2 interface.

Table 2.2 Experimental processes for QSSPC sample preparation

Step	Description	Chemical	Details
1	Cutting	--	Cutting EPR samples into 2.5×25 mm pieces with a diamond saw
2	Saw damage etch	HF:HNO_3 solution (1:10)	Remove saw damage from Si surface and edges (from cutting) by etching in HF:HNO_3 solution for 3 minutes.
3	HF dip	10% HF solution	Until hydrophobic to remove native oxide
4	RCA clean 1	5:1:1 H_2O:NH_4OH:H_2O_2 solution	For 10 minutes in warm solution (~80°C)
5	RCA clean 2	5:1:1 H_2O:HCl:H_2O_2 solution	For 10 minutes in warm solution (~80°C)
6	HF dip	Clean 10% HF solution	Until hydrophobic to remove native oxide
7	Oxidation	Oxygen	In TCA cleaned tube at 1000°C to grow ~50 nm oxide layers, followed by an insitu anneal in N_2 at the oxidation temperature for 30 minutes on selected samples.
7	Forming gas anneal (FGA)	Forming gas (5% H_2 in 95% Ar)	All samples receive FGA at 400°C for 30 minutes to hydrogenate the Si-SiO_2 interface
8	Rapid thermal anneal (RTA)	N_2	RTA at 800°C for 3 minutes to dehydrogenate the Si-SiO_2 interface.

Table 2.3 Experimental processes for EPR sample preparation

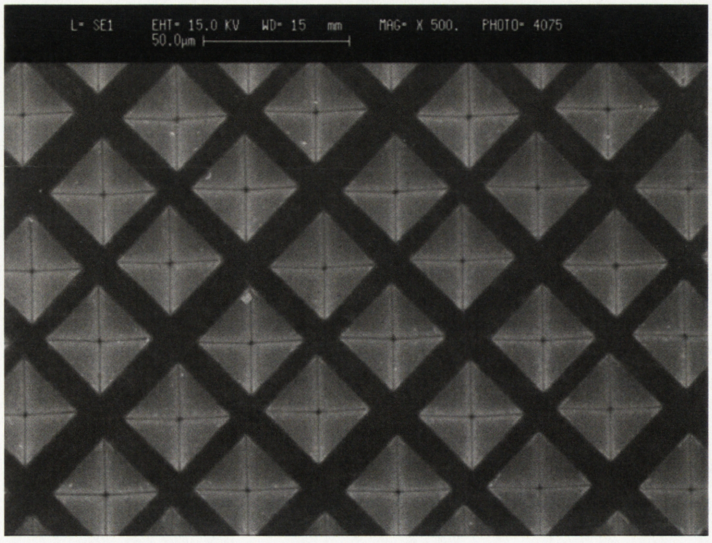

Figure 2.1 SEM picture of Si surface patterned and etched.

2.2.2 Dependence of Si-SiO_2 interface properties on oxidation and Si surface conditions

The Si-SiO_2 interface properties are influenced by the oxidation and Si surface conditions. Table 2.4 shows the fixed charge density Q_f and mid gap D_{it} for p MOS structures. The Si substrates had been etched in HF:HNO_3 solutions at different concentrations for 3 minutes before oxidation (1100°C in oxygen with TCA). No FGA was applied to the structures. The etch process does not significantly influence the charge density, however, it reduces the defect density, D_{it}.

HF:HNO_3 ratio	Q_f ($\times 10^{11}$ /cm^2)	Mid gap D_{it} ($\times 10^{10}$ cm^{-2}eV^{-1})
0	3.6	5.8
1:20	3.4	4.7
1:15	3.3	3.9
1:10	3.5	2.9

Table 2.4 Fixed charge density Q_f and mid gap D_{it} for p type Si/SiO_2 structure. The Si samples were etched in HF:HNO_3 solution before oxidation. 100 nm oxide was thermally grown at 1100°C in dry oxygen. No subsequent FGA was carried out. The error in both mid gap D_{it} and Q_f is estimated to be +/-10%

Table 2.5 shows the influence of oxidation temperature and addition of TCA on p type Si-SiO_2 interface properties. Etching in 15:1 HF:HNO_3 solution was performed for 3 minutes before oxidation. The addition of TCA results in water vapor in the oxidation furnace, enhancing the oxidation rate and fixed charge density, but has little influence on D_{it}. Raising the oxidation temperature generates a less stressed interface[68], resulting in lower interface defect density. These results are in agreement with other publications[35, 36].

Temperature (°C)	TCA on/off	Q_f ($\times 10^{11}$ /cm^2)	Mid gap D_{it} ($\times 10^{10}$ cm^{-2}eV^{-1})
1000	On	3.0	4.4
1000	Off	2.5	4.3
1100	On	3.3	3.9
1100	Off	2.8	3.7

Table 2.5 Fixed charge density Q_f and mid gap D_{it} for p type Si/SiO_2 structure, with the oxidation temperature and addition of TCA. No FGA was performed after oxidation.

Table 2.6 shows the influence of Si surface orientation on Q_f and D_{it}. (111) and (100) MOS structures were used. Etching in 1:15 HF:HNO_3 solution was performed before oxidation at 1000°C with TCA. For the same processing conditions, the (111) Si surface shows a higher D_{it} than the (100) Si surface.

Si surface orientation	Q_f ($\times 10^{11}$ /cm^2)	Mid gap D_{it} ($\times 10^{10}$ cm^{-2}eV^{-1})
100	3.0	4.4
111	2.3	66

Table 2.6 Fixed charge density Q_f and mid gap D_{it} for p type Si/SiO_2 structure, with Si surface orientation. No FGA was carried out after the oxidation.

2.2.3 Si-SiO_2 interface properties with insitu annealing in nitrogen

Post oxidation in-situ anneals in nitrogen or argon at high temperatures are known to be an effective method to improve the quality of the Si-SiO_2 interface following thermal oxidation. However, there appears to be not much experimental data supporting the improvement from insitu annealing. In this section, the influence of insitu annealing following oxidation on the Si-SiO_2 interface properties is discussed.

Figure 2.2 shows the effect of the in-situ N_2 anneal on lifetime measured directly after oxidation for p type Si/SiO_2 structures. The line with open circles represents oxidised wafers without in-situ anneal in N_2, while the line with open rectangle symbols represents wafers with in-situ N_2 anneal at the oxidation temperature for 30 minutes. The effective lifetime for the oxidized sample with in-situ N_2 anneal is higher than the oxidized sample without in-situ N_2 anneal at all injection levels. The bulk lifetime for both samples should be the same, therefore, the difference in the effective lifetime must be due to a difference in surface passivation. Clearly oxidation with an insitu N_2 anneal results in a better passivated surface.

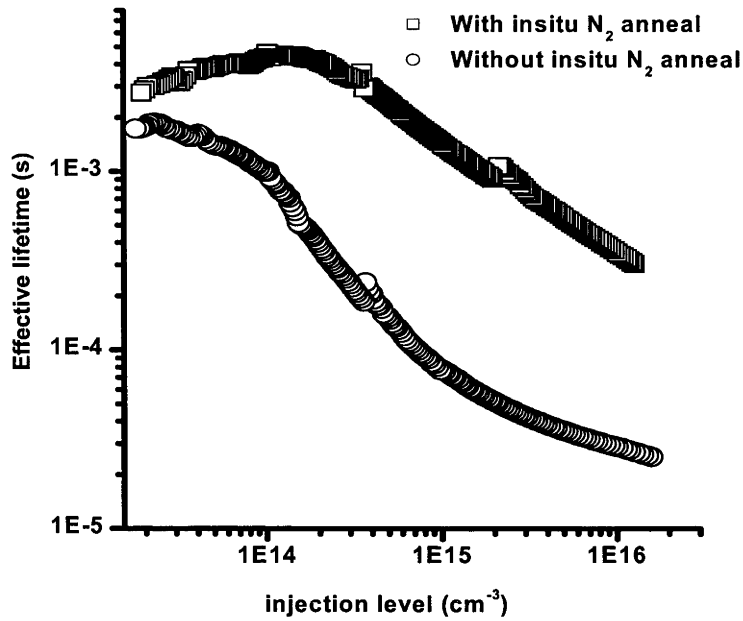

Figure 2.2 Effective lifetime vs injection level. Comparison between Si/SiO_2 structures with insitu annealing in N_2 and without insitu anneal. 50 nm oxide was grown on both sides at 1000°C in dry oxygen. No FGA was carried out after oxidation.

The influence of post oxidation insitu N_2 anneal on the thermal stability of SiO_2/Si structures was also studied. After FGA, all samples received RTA treatments. The effective lifetime was measured and from this, the effective surface recombination velocity calculated according to equation (1.13), assuming infinite bulk lifetimes.

The surface recombination velocity S_{eff} at the injection level of $1.5\times10^{14}/cm^2$ after various thermal processes is shown in figure 2.3. 'As oxidized' represents values measured just after oxidation. 'FGAed' represents the values following forming gas annealing. 'RTA1' and 'RTA2' were performed at 500°C for 3 minutes and 600°C for 3 minutes in N_2 gas respectively. All of the (100), (111) and textured orientations display the same trend. After oxidation, samples with in-situ N_2 anneal have lower recombination velocity. The FGA process introduces hydrogen to the Si-SiO_2 interface and lowers S_{eff}. 'RTA1' increases S_{eff}. The difference between samples with and without in-situ N_2 anneal is small at these two steps. As samples were FGAed, the majority of dangling bonds at the interface are passivated with hydrogen. An RTA at 500°C for 3 mins does not lead to a significant release of hydrogen from the interface. However, after RTA2, a significant fraction of hydrogen has been driven away from the Si-SiO_2 interface. A bigger difference in S_{eff} between samples with and without in-situ N_2 anneal is apparent. At this stage, the in-situ annealed samples have only around half the S_{eff} values of the samples without in-situ anneals. The in-situ N_2 annealing improves the thermal stability of the Si-SiO_2 interface.

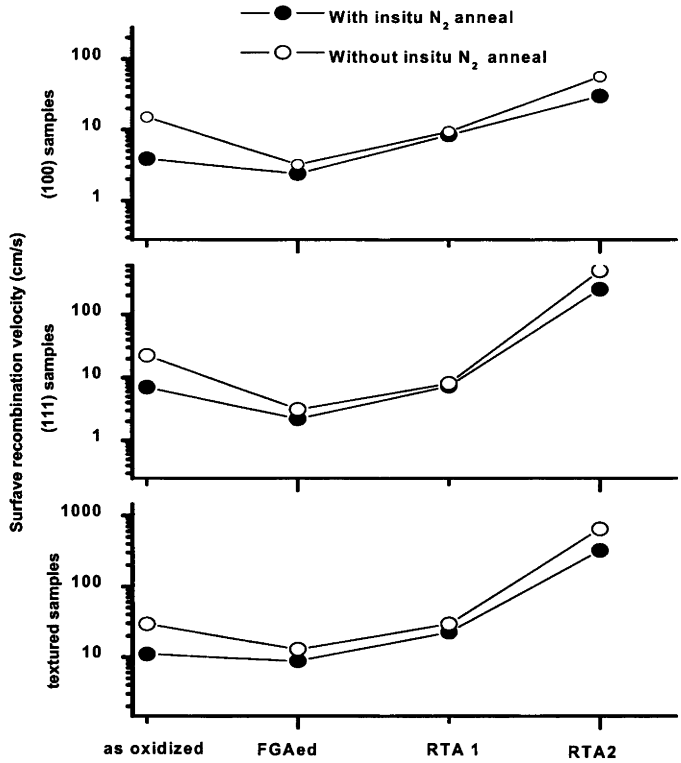

Figure 2.3 Comparison of surface recombination velocity for SiO_2/Si structures with and without insitu annealing in N_2

2.2.4 Hydrogenation and dehydrogenation of Si-SiO_2 interface

Figure 2.4 shows a comparison of CV curves between an as grown Si-SiO_2 interface and an FGAed Si-SiO_2 interface. The flat band voltages for the as oxidized and FGAed MOS structures are -1.53 V and -1.25 V, respectively. The calculated values for the fixed interface charge density are $+3.1\times10^{11}$ cm^{-2} and $+2.5\times10^{11}$ cm^{-2}, respectively. A larger stretch out between QSCV and HFCV curves is observed for the as grown Si-SiO_2 interface, demonstrating a higher interface defect density[16]. The mid gap defect density for as oxidized samples is about 4.3×10^{10} $cm^{-2}eV^{-1}$ and for FGAed samples it is about 7.9×10^{9} $cm^{-2}eV^{-1}$. Hydrogenation using an FGA effectively reduces the Si-SiO_2 interface density of electrically active defects. The lowest detected mid gap D_{it} by the author is about $2\text{-}3\times10^{9}$ $cm^{-2}eV^{-1}$, when the oxide samples were extremely processed and FGAed. The FGA also results in a slight reduction in Q_f, as evidenced by a reduction in the flat band voltage. This is likely to be the result of the passivation of a percentage of the charged oxide defects responsible for the measured Q_f, in a similar way to the passivation of the interface defects by the FGA."

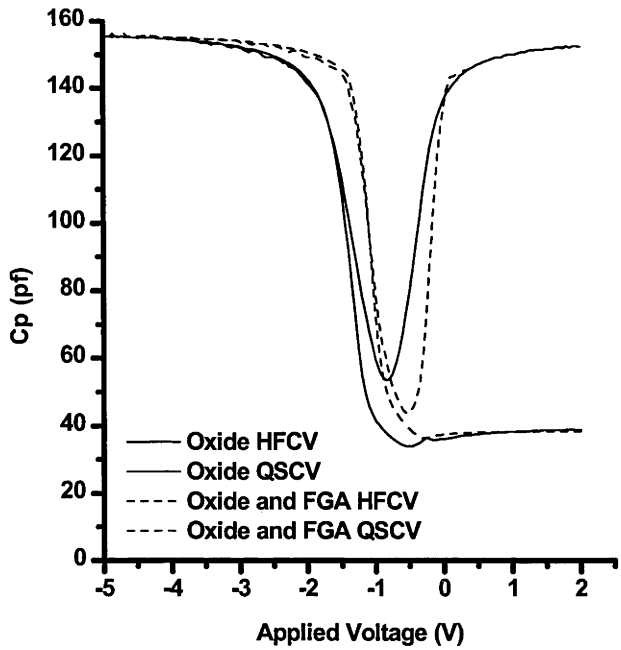

Figure 2.4 High Frequency CV (HFCV) curves and Quasi Static CV (QSCV) curves for SiO_2/Si structures with and without FGA. 100 nm oxide was grown at 1000°C in dry oxygen.

Stesmans and his co-workers examined the influence of thermal annealing on the Si-SiO_2 interface defect properties by EPR measurements. Their work mainly focussed on P_b centers, the paramagnetic defects at the Si surface. P_b centres become electrically and paramagnetically inactive by bonding with hydrogen. The passivation of P_b centres by hydrogen depends strongly on temperature and time. Normally annealing at 400°C to 450°C for 10 to 60 minutes results in lowest P_b density[74, 76]. Higher temperature annealing in molecular hydrogen results in the generation of additional P_b centres[74, 76]. Above 550°C, annealing in molecular hydrogen introduces more interface damage than annealing in vacuum [77], probably because of the atomic hydrogen generated at high temperature. Annealing in molecular hydrogen above 550°C also introduces additional interface positive charges[78, 102], which is speculated to be due to the forming of $(H_3O)^+$ hydronium ions.

Figure 2.5 shows the EPR spectra of the Si/SiO_2 structures (oxide thickness of 50 nm) after RTA at 800°C for 3 minutes in N_2 flow (black lines). As a reference, the Si/SiO_2 samples were also measured before RTA (red lines). Figure 2.5(a) was measured with the magnetic field parallel to (111) direction, while figure 2.5(b) was measured with the magnetic field perpendicular to (111).

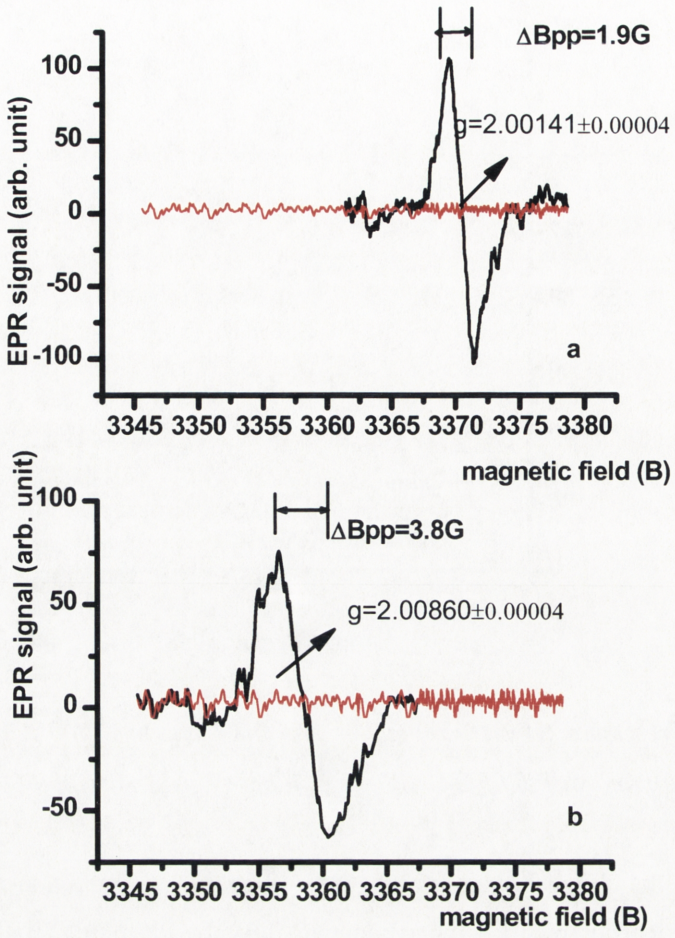

Figure 2.5 EPR spectrum for SiO_2/Si obtained when magnetic field is parallel to (111) direction (2.5(a)) and perpendicular to (111) direction (2.5(b)). The black lines represent samples with RTA while the red lines represent samples without RTA.

The g value has the following relationship with the angle θ between magnetic field direction and (111) direction:

$$g(\theta)=[(g_{//}\cos(\theta))^2+(g_{\perp}\sin(\theta))^2]^{1/2} \qquad (2.5)$$

where $g_{//}$ and $g_{\perp}$ represent the g value measured when the magnetic field is parallel and perpendicular to (111) direction, respectively.

EPR measurements were carried out to investigate the influence of post oxidation insitu annealing on the Si-SiO_2 interface defect density. The results indicate that the post oxidation in-situ N_2 anneal leads to a significant reduction in the P_b centre density measured after RTA at 800°C in N_2 for 3 minutes, with a P_b density of 4.6×10^{12} /cm^2 for a sample with in-situ anneal compared with 8.0×10^{12} /cm^2 without an anneal.

2.2.5 Comparison between hydrogenated and dehydrogenated SiO_2/Si structures by Lifetime-Voltage measurements

Lifetime-voltage measurements were conducted to compare hydrogenated and dehydrogenated SiO_2-Si interfaces. The oxide layers were grown at 1000°C in dry oxygen with insitu annealing in N_2. The oxide thickness was 50 nm. Note that no diffusion was performed on these samples. As discussed in section 1.2.1, Joe can be extracted from lifetime measurements even in the absence of diffusion, if the sample surface is accumulation or inversion. Hydrogenation was realized by forming gas annealing at 400°C for 30 minutes. Dehydrogenation was realized by rapid thermal annealing in dry N_2 at 500oC for 10 seconds. This treatment results in partial removal of hydrogen from the interface.

Figure 2.6 shows the lifetime results and figure 2.7 shows the J_{oe} results. Both lifetime and J_{oe} are measured simultaneously from the 50 nm SiO_2/Si structures. At all bias voltages, the lifetime for the hydrogenated sample is higher and the J_{oe} is lower than the dehydrogenated samples. Especially at inversion and accumulation regions when lifetime saturates with voltage bias, the difference between the two structures is obvious. However, the bulk lifetimes for the two structures are calculated to be nearly the same (the calculation was shown in section 1.2.2, using equation 1.14), demonstrating that the thermal processes only affect the electrically active interface defect density and no bulk damage is introduced.

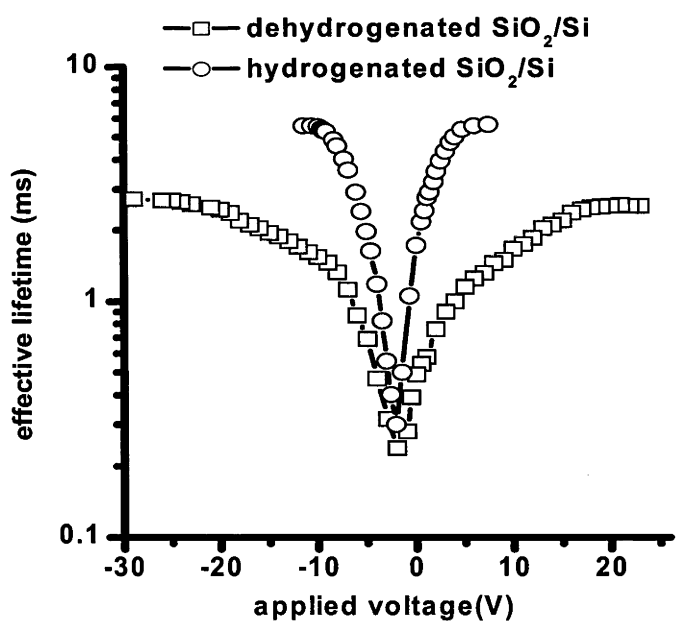

Figure 2.6Effective lifetime with applied bias comparison between hydrogenated (by FGA) and dehydrogenated (by 500°C RTA for 10 seconds) SiO_2/Si structures

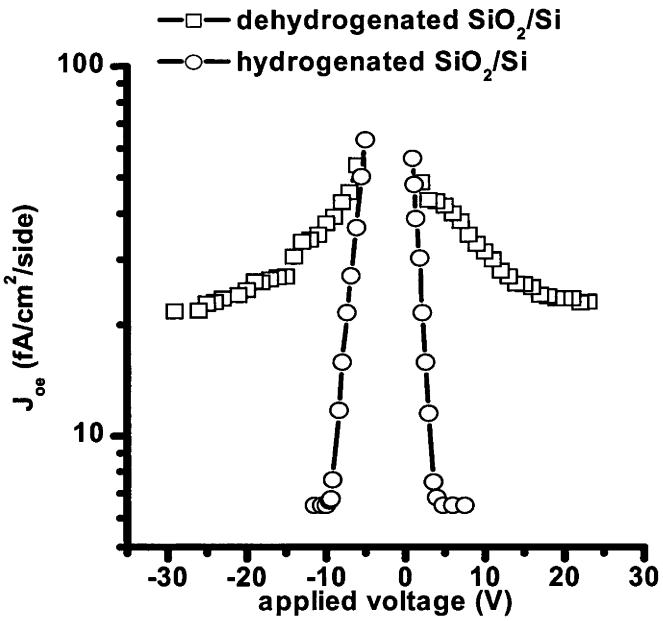

Figure 2.7 J_{oe} with applied bias comparison between hydrogenated (FGA) and dehydrogenated (by 500°C RTA for 10 seconds) SiO_2/Si structures

2.3 Comparison of the interface properties of (100), (111) and textured Si surfaces

The Si-SiO_2 interface properties depend, among other factors, on the crystal orientation. In general, (111) oriented surfaces are more difficult to passivate than (100) surfaces. (111) surfaces always display a larger value for the interface trap density D_{it} than (100) surfaces[72, 101]. Texturing provides good optical properties for solar cells but may decrease the achievable degree of surface passivation by increasing the surface area and by exposing crystal planes that are inherently more difficult to passivate.

2.3.1 Experimental details

For CV measurements, p/B, (100), 10-23 Ωcm, Cz, ~500 μm thick wafers and n/P, (111), 3-10 Ωcm, Cz, ~500 μm wafers were used. For QSSPC measurements, p type, (100), FZ, >100 Ωcm, 550 μm wafers and n type, (111), FZ, ~100 Ωcm, 550 μm wafers. Treatments to the CV and PCD samples are listed in table 2.7 and 2.8, respectively. Phosphorus diffusions were carried out on some samples for J_{oe} measurements. The experimental procedure is shown in figure 2.8. The sheet resistance for (100) p type samples is shown in figure 2.9.

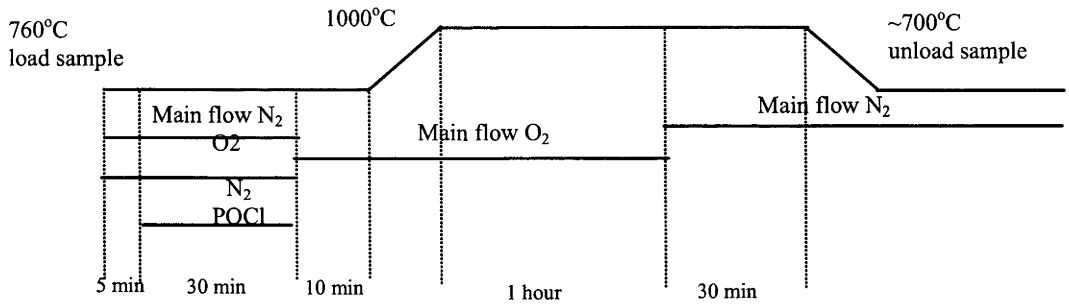

Figure 2.8. Experimental procedure for phosphorus diffusion

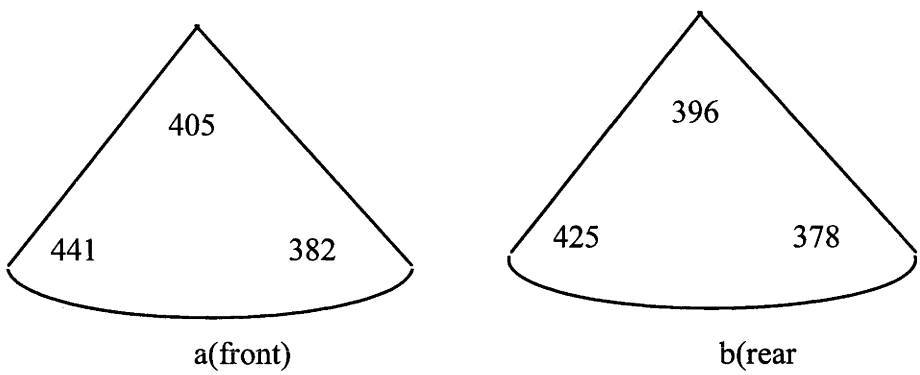

Figure 2.9 resistivity of p type (100) sample (a) front side and (b) rear side followed the recipe shown in figure 2.8.

After oxidation and insitu annealing in N_2 gas, the resistivity is around 382-441 Ω/□ for p type (100) Si samples and 270-275 Ω/□ for n type (111) samples. Figure 2.10 (a) (b) and (c) show the cross section of the samples after texturing, 3 minutes etching and 9 minutes etching, respectively. The inverted pyramid depth in figure 2.10 (a) is 20 μm. The scale of all three figures is consistent with the scale in figure 2.10(c).

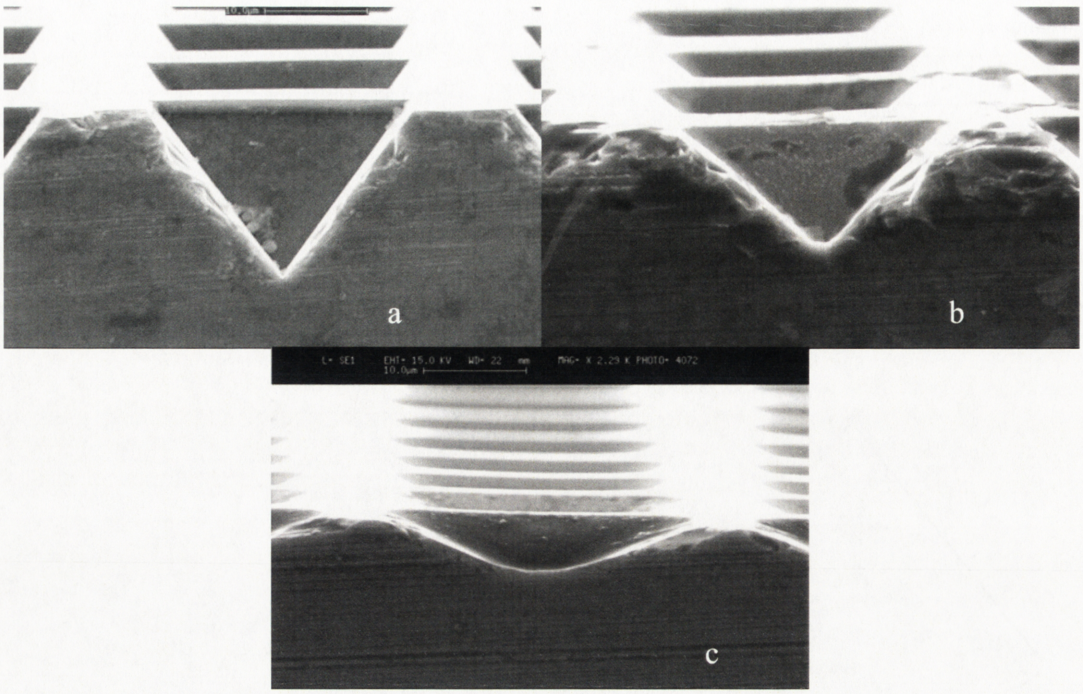

Figure 2.10 the cross section of the Si samples after texturing (a), 3 minutes etching (b) and 9 minutes etching (c), respectively.

Step	Description	Chemical	Details
1	Saw damage etch	$HF:HNO_3$ solution (1:10)	Remove saw damage from Si surface and edges by etching in $HF:HNO_3$ solution for 3 minutes.
2	HF dip	10% HF solution	Until hydrophobic to remove native oxide
3	Cleaving	--	(100) Wafers were cleaved into quarters and labelled.
4	RCA clean 1	5:1:1 $H_2O:NH_4OH:H_2O_2$ solution	For 10 minutes in warm solution (~80°C)
5	RCA clean 2	5:1:1 $H_2O:HCl:H_2O_2$ solution	For 10 minutes in warm solution (~80°C)
6	HF dip	Clean 10% HF solution	Until hydrophobic to remove native oxide
7	Oxidation	Oxygen	In TCA cleaned tube at high temperature to grow ~100 nm oxide layers, followed by an insitu anneal in N_2 at the oxidation temperature for 30 minutes.
8	FGA	Forming gas (5% H_2 in 95% Ar)	FGA at 400°C for 30 minutes to hydrogenate the Si-SiO_2 interface
9	RTA	N_2	RTA at temperature from 500°C to 800°C in N_2
10	One side oxide remove	HF fume	One side of oxide was removed by HF fume
11	Al deposition	Al	At high vacuum ($<3\times10^{6}$torr), ~80 nm thick Al was deposited on oxide layer through a shadow mask with area of 4.7×10^{-3} cm^2

12	Ohmic contact	Ga-In	Ohmic contact by Ga-In paste on oxide removed Si side.

Table 2.7 Experimental processes for CV sample preparation

Step	Description	Chemical	Details
1	Quartering	---	For (111) samples, wafers were cut by a diamond saw into quarters and labelled.
2	Saw damage etch	HF:HNO_3 solution (1:10)	Remove saw damage from Si surface and edges by etching in HF:HNO_3 solution for 3 minutes.
3	HF dip	10% HF solution	Until hydrophobic to remove native oxide
4	Texturing	TMAH	Some (100) QSSPC samples were patterned and textured to form inverted dots in alkali solution, the SEM picture of the textured surface is shown in figure 2.1.
5	Etching	HF:HNO_3 solution (1:10)	Some textured samples were etched to form surface orientation between (100) and textured surface.
6	Cleaving	--	(100) Wafers were cleaved into quarters and labelled.
7	(Radio Corporation America) RCA clean 1	5:1:1 H_2O:NH_4OH:H_2O_2 solution	For 10 minutes in warm solution (~80°C)
8	(Radio Corporation America) RCA clean 2	5:1:1 H_2O:HCl:H_2O_2 solution	For 10 minutes in warm solution (~80°C)
9	HF dip	Clean 10% HF solution	Until hydrophobic to remove native oxide
10	P diffusion and oxidation	POCL	Light phosphorus diffusion and oxidation to QSSPC samples. Receipt is shown in figure 3.6.
11	FGA	Forming gas (5% H_2 in 95% Ar)	FGA at 400°C for 30 minutes to hydrogenate the Si-SiO_2 interface
12	RTA	N_2	On selected samples, RTA at temperature from 500°C to 800°C in N_2
13	Vacuum anneal	Vacuum	On selected samples vacuum annealing at 800°C for 2 hours.

Table 2.8 Experimental processes for QSSPC sample preparation

2.3.2 Comparison of Si-SiO_2 interface properties under hydrogenated and dehydrogenated conditions

Si-SiO_2 interface properties were investigated under hydrogenated and dehydrogenated conditions. (100) and (111) oriented Si structures were compared. The vacuum annealing was realized at the pressure of 1×10^{-6} Torr for 2 hours at other where. The RTA was realized at

atmosphere pressure for 3 minutes in our lab. J_{oe} values for hydrogenated and dehydrogenated samples are summarized in table 2.9. The (111) Si surface has a higher recombination velocity than the (100) Si surface at the hydrogenated and dehydrogenated stages. At 800°C, vacuum annealing may dehydrogenate the Si-SiO_2 more completely than RTA, rendering higher J_{oe} values for both the (100) and the (111) silicon. The RTA in N_2, while not producing complete dehydrogenation, results in substantial dehydrogenation and is used subsequently in the thesis.

	FGAed	Vacuum anneal	RTA
(100) Si/SiO_2 (fA/cm^2/side)	6.5	2.5×10^2	1.8×10^2
(111) Si/SiO_2 (fA/cm^2/side)	20	2.8×10^3	1.4×10^3

Table 2.9 J_{oe} values for (100) and (111) Si/SiO_2 structures at hydrogenated and dehydrogenated stages.

Figure 2.11 shows the D_{it} distribution within the Si forbidden bandgap for both (111) and (100) oriented MOS structures. Both MOS structures received a FGA before oxide removal. The (111) MOS shows higher D_{it} than (100), especially around midgap(0.55eV).

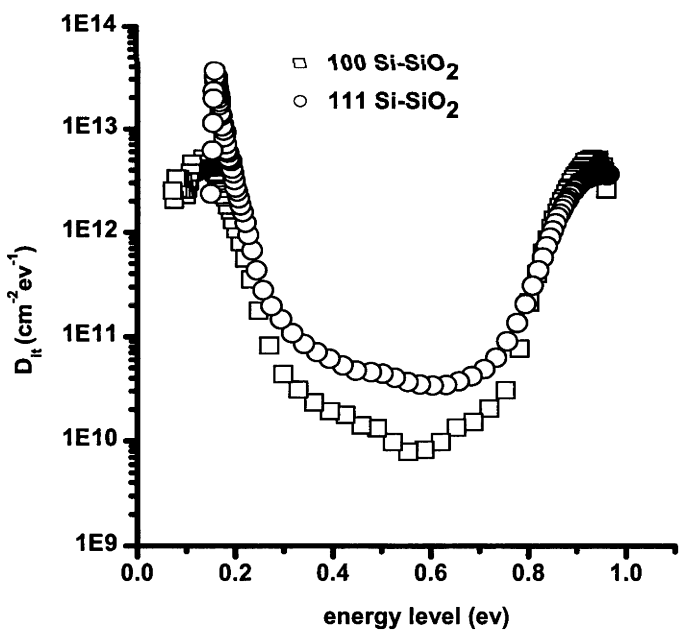

Figure 2.11. D_{it} distribution within Si forbidden bandgap for FGAed (111) and (100) MOS structures. 100 nm oxide was thermally grown at 1000°C followed by insitu annealing in N_2.

2.3.3 Influence of Si surface orientation on the thermal stability of the Si-SiO_2 interface

The thermal stability of oxidised Si samples is of importance where such wafers undergo subsequent thermal treatments in a hydrogen free atmosphere. This is the case, for example, when silicon nitride is deposited on oxidised Si samples, as will be discussed in subsequent chapters.

The thermal stability of (100), (111) and textured Si surfaces in SiO_2/Si structures is investigated by means of QSSPC and CV measurements. Some textured samples were etched in 10:1 HF:HNO_3 solution to form a Si surface structure between textured and (100) planar surface. RTA in N_2 was carried out subsequently to remove hydrogen from the Si-SiO_2 interface. Effective lifetime and J_{oe} were measured. For undiffused samples, the surface recombination velocity was determined using equation (1.13).

Figure 2.12 (a) and (b) show the surface depassivation process of both undiffused and phosphorus diffused samples. Isothermal anneals were done at 550°C for 30 to 360 seconds in nitrogen. On all samples, the rate of increase of S_{eff} or J_{oe} decreases with increasing anneal time. The (100) surface shows the lowest surface recombination velocity and depassivation rate, while textured wafers display the most rapid depassivation. The depassivation rates of the etched samples are between those of the textured samples and the (100) samples.

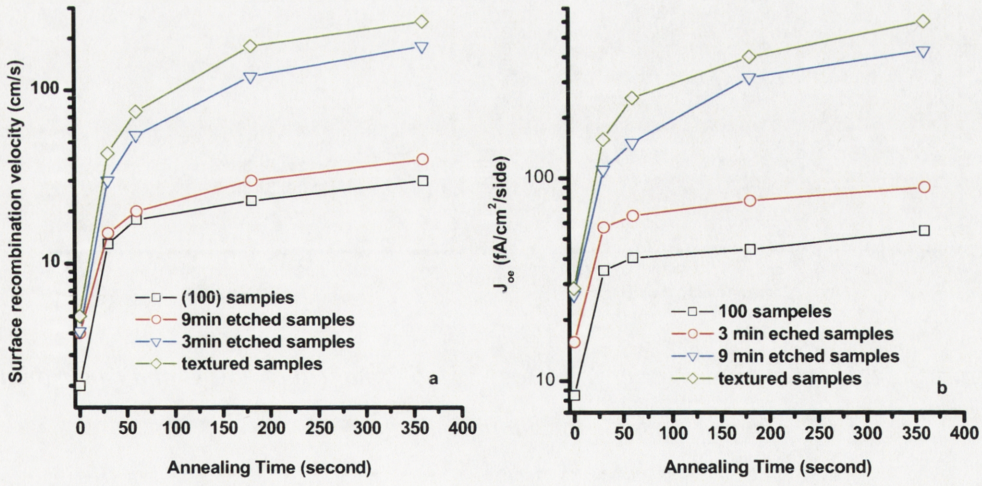

Figure 2.12: Effective surface recombination velocity S_{eff} (a) and emitter saturation current J_{oe} (b) vs isothermal annealing time for RTAs at 550°C

Figures 2.13 (a) and (b) show the isochronal RTA results. All samples were annealed for 3 minutes in nitrogen. For all the samples, the depassivation rate increases with annealing temperature. Similar to Figures 2.12, (100) samples display the slowest isochronal depassivation rate while textured wafers display most rapid depassivation.

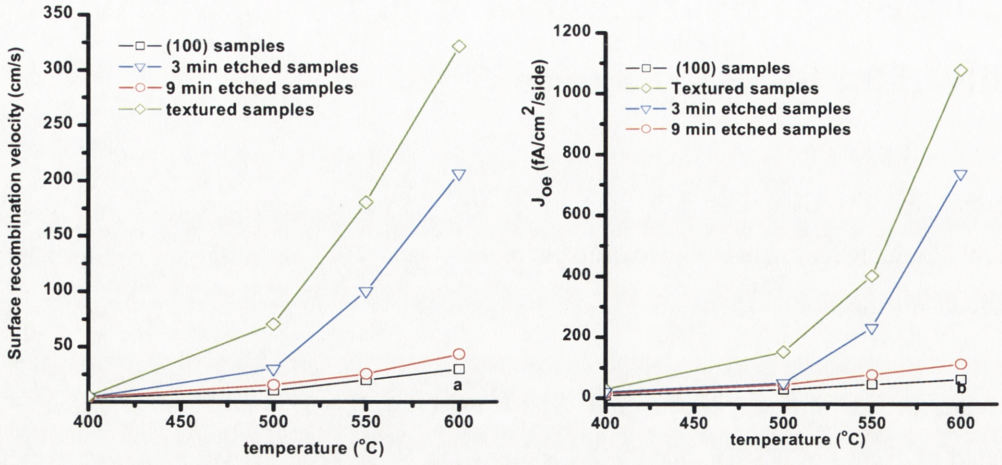

Figure 2.13: Effective surface recombination velocity S_{eff} (a) and emitter saturation current J_{oe} (b) vs isochronal annealing temperature for 3 min RTAs

Figure 2.14 compares the thermal stability of (100) and (111) Si surfaces of SiO_2/Si structures. Figure 2.14 (a) shows the thermal stability under isothermal annealing at 550°C and figure 2.12 (b) shows the thermal stability under isochronal annealing for 3 minutes.

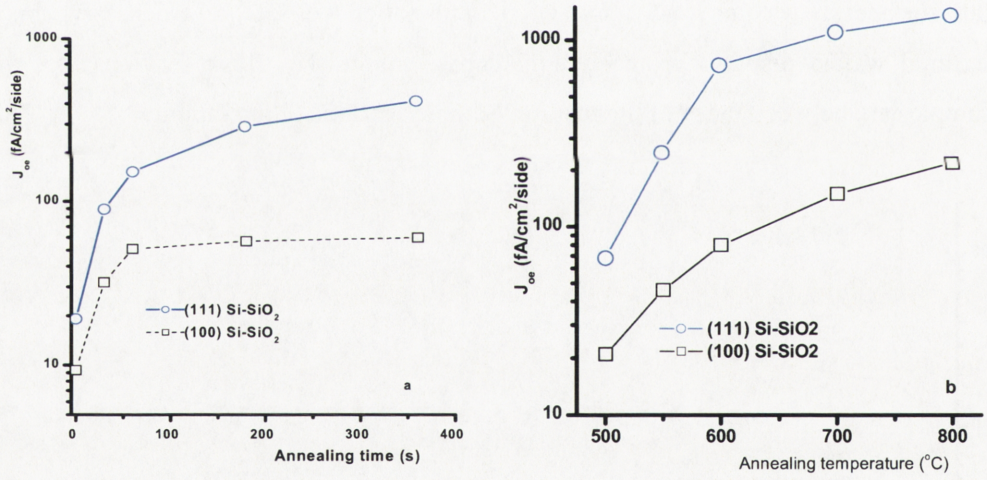

Figure 2.14. Emitter saturation current Joe vs isothermal (a) at 550°C and isochronal (b) anneals for 3 min RTAs in N_2

Figure 2.15 shows the HFCV and QSCV curves following RTA treatments at 550°C. With increasing anneal time, the value of the flat band voltage becomes more negative and a greater stretch out between HFCV and QSCV curves is observed, indicating that more interface defects and charges are generated during the isothermal annealing. Figure 2.16 compares the RTA isothermal annealing effects to the mid gap D_{it} (a) and charge density (b) for (111) and (100) Si structures. Table 2.10 summarizes the comparison of mid gap D_{it} and charges density for (111) and (100) Si structures, following isochronal RTAs for 3 minutes in N_2.

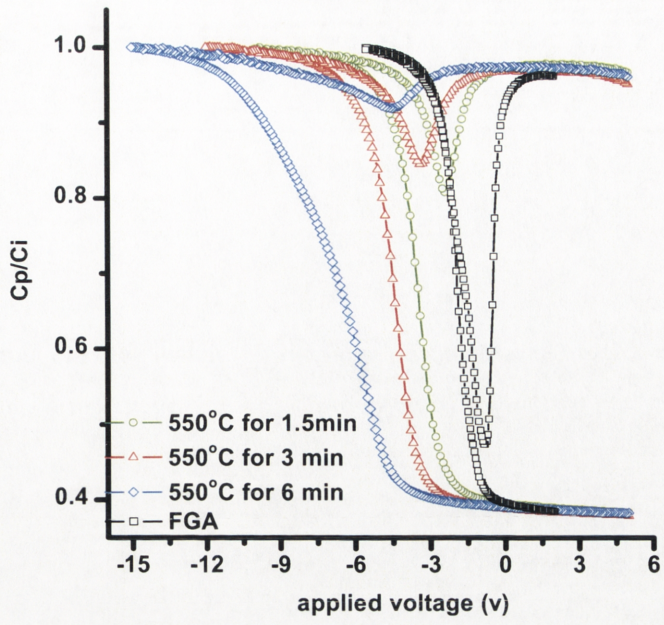

Figure 2.15. HFCV and QSCV curves for (111) SiO_2/Si structures after FGA and RTA at 550°C for 1.5 to 6 minutes.

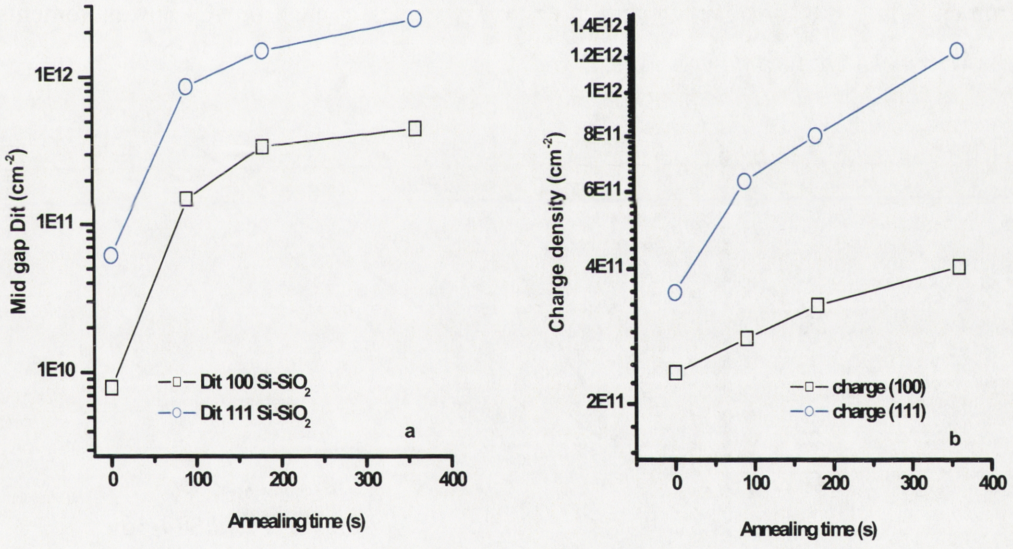

Figure 2.16. Mid gap D_{it} (a) and charge (b) density vs isothermal anneal at 550°C RTAs in N_2

(111) surfaces display a higher defect density and charge density than (100) surfaces, and show a more rapid depassivation rate. Some of the parameters (charge density for (111) Si surface after 800°C RTA and defect density for (111) Si surface after 700°C and 800°C RTA) in table 2.10 could not be obtained since they are beyond the measurement limit of the equipment.

	(100) Si-SiO_2		(111) Si-SiO_2	
	Q_f ($\times 10^{11}$ cm^{-2})	Mid gap D_{it} ($\times 10^{11}$ cm^{-2}eV^{-1})	Q_f ($\times 10^{11}$ cm^{-2})	Mid gap D_{it} ($\times 10^{11}$ cm^{-2}eV^{-1})
550°C	3.3	3.4	8.0	15
600°C	7.2	7.1	22	30
700°C	13	18	52	-
800°C	19	26	-	-

Table 2.10. Comparison of mid gap D_{it} and charges density for (111) and (100) Si structures, following isochronal RTAs for 3 minutes in N_2.

2.3.4 Relationship between J_{oe} and D_{it}

Both J_{oe} and D_{it} are indicators of Si surface passivation. Figure 2.17 shows the relationship between J_{oe} and D_{it}. All samples have a 50 nm thick oxide. For each data point, the J_{oe} value comes from the QSSPC measurements on phosphorus diffused high resistivity (>100 Ωcm) samples, while the mid gap D_{it} and average D_{it} values come from CV measurements on low resistivity (~15 Ωcm) p type samples.

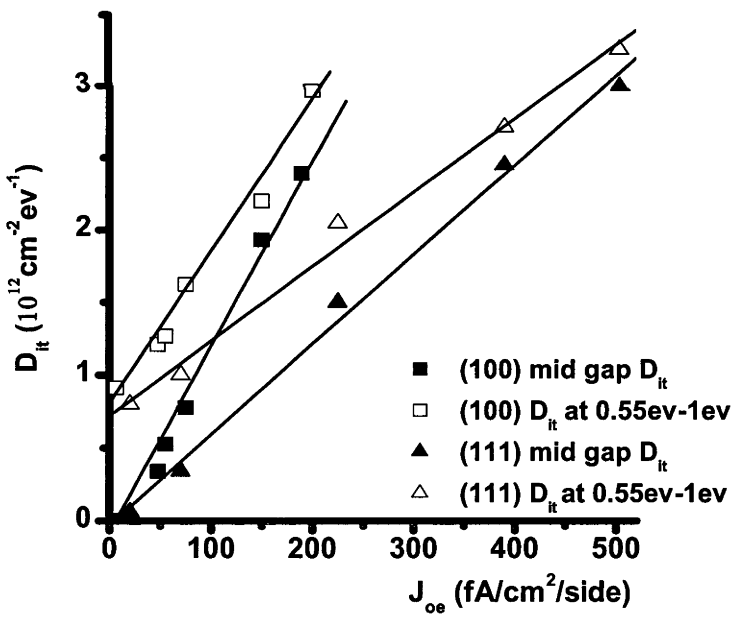

Figure 2.17 . Relationship between D_{it} and J_{oe}. The oxide thick is 50 nm for all samples. The J_{oe} and D_{it} were increased by thermal treatments.

The most striking feature of this figure is that both the average defect density and mid gap D_{it} have a linear relationship with J_{oe} for both (100) and (111) Si-SiO_2 interfaces. In particular, the mid gap D_{it} is proportional to J_{oe}. The mid gap D_{it} value is therefore a good indicator of surface passivation.

The linear fit for mid gap D_{it} nearly travels through the origin, indicating that if surface recombination is zero, the mid gap defect density is also negligibly low. However, the positive intercept for the linear fit of the average defect density may indicate that some of the interface defects near the band edges are not highly recombination active.

The different slopes of the linear fits for the (111) and the (100) samples could have several origins. One interpretation is that the higher J_{oe} (for a given D_{it}) for (111) samples indicates a greater 'average' capture cross section of the defects on the (111) Si-SiO_2 interface. However, the measured value of J_{oe} also depends sensitively on the surface doping concentration. In principle, a higher surface P concentration for the (100) samples by a factor of 2 or more could also explain the different slopes. The diffusions for the (111) and (100) samples were carried out using the same diffusion recipe. Figure 2.18 shows typical spreading resistance profiles. The P profile for the (100) sample shows some dopant depletion close to the surface, the origin of which is not known. However, it can be concluded from these profiles that the surface P concentration for the (100) samples is not greater than that for the (111) samples by a factor of 2 or more.

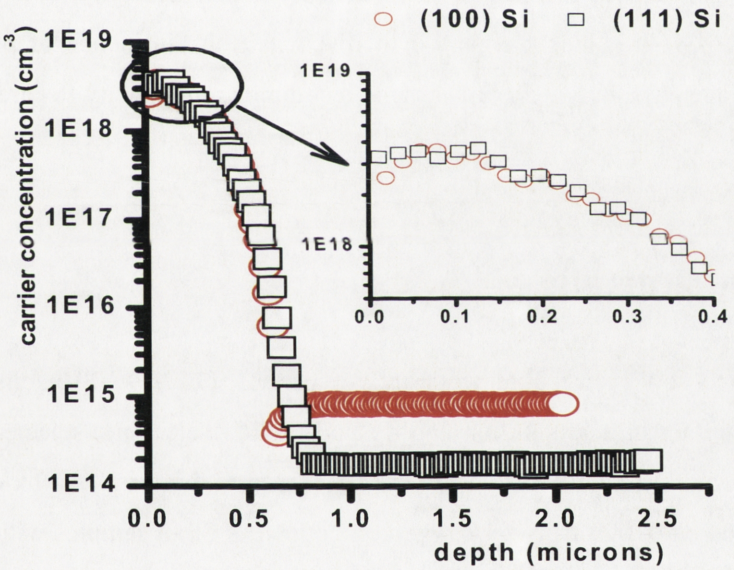

Figure 2.18. carrier concentration profile of P diffusion in (100) and (111) Si

The relationship between D_{it} and J_{oe} in figure 2.17 needs to be interpreted with caution, since the D_{it} and J_{oe} results come from quite different samples – the former from undiffused, moderate resistivity Cz samples, and the latter from diffused, high resistivity FZ samples.

2.4 Influence of Phosphorus Diffusion on the Si surface passivation of SiO_2/Si structures

Phosphorus diffusion for the formation of n^+ emitters is one of the critical steps in fabrication of most solar cells. It is well known that P diffusion can improve surface passivation by reducing the surface concentration of holes and thus lowering the overall carrier recombination rate. However, P diffusions can also lead to a decrease in passivation through additional recombination in the n^+ emitter. This is particularly significant for heavily doped emitters. In addition, it is thought that the defect density at the Si-SiO_2 interface increases above a certain substrate doping level [1]. However, there appears to be little data which could be used to confirm or reject this hypothesis. This is chiefly due to the fact that heavily doped, diffused surfaces are more difficult to analyse than lowly or moderately doped surfaces.

In this section, SiO_2/Si structures were used to investigate the influence of phosphorus diffusions on the Si surface passivation. J_{oe} and surface recombination velocity (S) are extracted and compared for each structure.

2.4.1 Experimental details

Samples used for lifetime-voltage measurements are p type, FZ, (100), >100 Ω/cm, 500 μm thick Si wafers. After etching in acid solution and a standard RCA cleaning, selected samples received a light phosphorus diffusion (~300-400 Ω/□ after thermal drive in). An oxide around 50 nm was thermally grown at 1000°C in dry oxygen on both sides of all samples with an insitu anneal in nitrogen, followed by annealing in forming gas at 400°C for 30 min. ~5 nm Al was thermally evaporated on both sides of all samples. HF solution was used to open the window for Si bulk connecting. Bulk connection is realized by GaIn paste.

2.4.2 Influence of phosphorus diffusion on Si surface passivation

Figure 2.19 shows the modeled effect of surface charge on the surface minority carrier concentration in thermal equilibrium for two different substrate doping levels – one, a lightly

doped substrate (p type, 10^{14} cm^{-3}), the other, a heavily doped substrate (p type, 10^{18} cm^{-3}). Bandgap narrowing was included in the calculation of the minority carrier concentration.

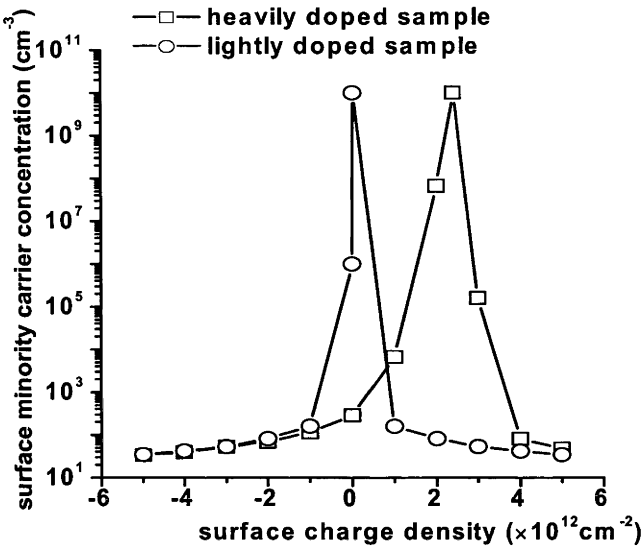

Figure 2.19. Surface minority carrier concentration in thermal equilibrium as a function of surface charge density for a lightly doped (blue, solid line) and heavily doped (pink, dashed line) substrate

In both cases, the minority carrier concentration displays a sharp peak for a given value of surface charge density and then rapidly decreases. On the left side of the peak, minority carriers are electrons (accumulation) while on the right side they are holes (inversion). As expected, the peak for the heavily doped sample occurs at a significant positive surface charge density which acts to repel the holes just beneath the insulator, while for a lowly doped sample the peak occurs for a low surface charge density. For large values of surface charge density, the surface minority carrier concentration saturates and becomes only weakly dependent on surface charge density, and nearly independent of substrate doping (particularly in accumulation). This implies that measurement of the emitter saturation current density J_{oe} at high surface charge densities, particularly in accumulation, can be used to detect any differences in interface defect properties, provided that differences in recombination in the emitter itself can be accounted for.

Figures 2.20 shows the effective lifetime and J_{oe} values for SiO_2/Si structure from the lifetime-voltage measurements. The lifetime voltage results are in good agreement with those of corona charging experiments[103, 104].

In accumulation (positive bias) the undiffused structures show a higher lifetimes and lower J_{oe} values than the phosphorus diffused samples.

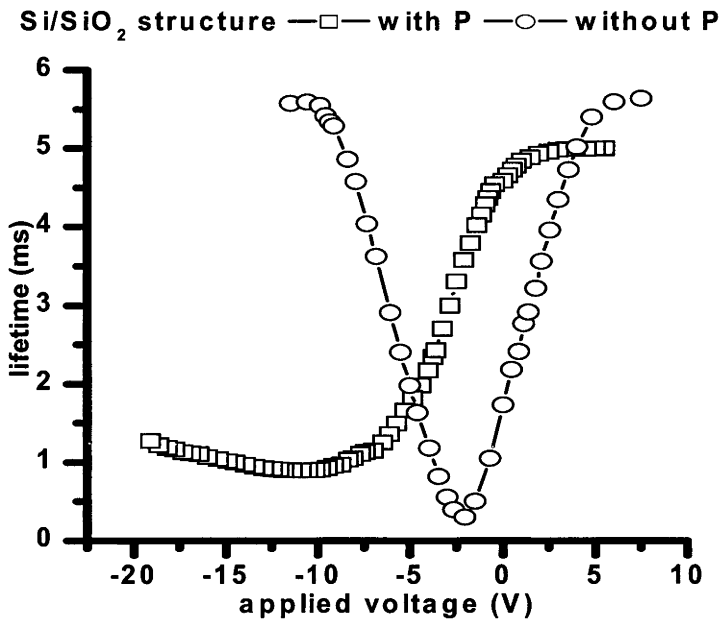

Figure 2.20: a) lifetime vs applied voltage for SiO_2/Si structure with vs without lightly P diffusion. The oxide is 50 nm. The sheet resistance for P diffused sample is around 400 Ω/□.

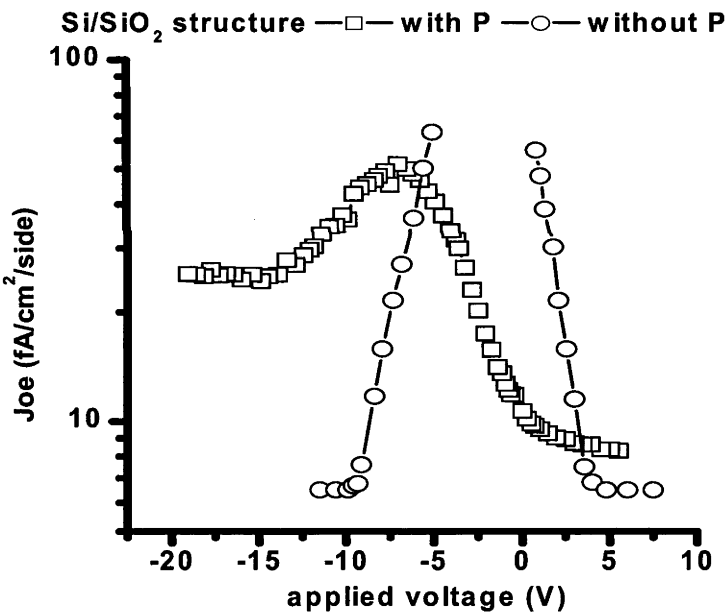

Figure 2.20 (b) J_{oe} lifetime vs applied voltage for SiO_2/Si structure with vs without lightly P diffusion. The oxide is 50 nm. The sheet resistance for P diffused sample is around 400 Ω/□.

In inversion, the lifetime curve for SiO_2/Si structure does not increase, probably due to a high leakage current (up to 20 mA) observed at high negative applied voltages. A high leakage current may introduce a voltage drop at the Si /metal contacts or across the Si bulk, making the measurement results difficult to interpret. Samples with oxide/nitride stacks display much low leakage currents (in the micro amp range). These results will be presented in next chapter.

Table 2.11 shows the corresponding effective surface recombination velocities of the samples in accumulation and inversion at the injection level used for the measurements (4×10^{15} cm^{-3}), calculated from the J_{oe} values.

	S at accumulation (cm/s)		S at inversion (cm/s)	
	With P	Without P	With P	Without P
SiO_2/Si	--	1.7	2.4	1.7

Table 2.11 surface recombination velocity from accumulation and inversion for SiO_2/Si structures. The determination of recombination velocity is described in section 1.3.2.

The difference in J_{oe} between diffused and undiffused samples will be partly due to emitter recombination in the diffused samples. In fact, modelling suggests that the small difference in J_{oe} for the oxide only sample can be explained on the basis of the additional contribution of the emitter alone (~2 fA/cm^2/side). Thus, for the oxidised, hydrogen passivated samples and the light phosphorus diffusions used here, it can be concluded that any increase in defect density resulting from the diffusion is not significant in terms of its effect on surface recombination.

2.5 Summary

Capacitance voltage, quasi steady state photoconductance and electron paramagnetic resonance measurements were combined to study the Si-SiO_2 interface electrical properties of thermally grown SiO_2/Si structures.

The Si-SiO_2 interface properties depend on the oxide growth conditions. A higher oxidation temperature normally results in a lower interface defect density. The Si-SiO_2 interface properties with a post oxidation in situ anneal in N_2 gas at the oxidation temperature are superior to the interface without insitu anneal in N_2 gas, as demonstrated by a higher effective lifetime and lower Si surface recombination velocity after FGA, a better thermal stability, and a lower Si interface paramagnetic defect density shown by EPR measurements.

Si-SiO_2 interface properties depend strongly on the Si surface orientation. The (111) Si surface shows a much higher recombination velocity, interface defect density (especially around the mid bandgap) and fixed positive charge density than the (100) Si surface at the hydrogenated stage. The (111) Si-SiO_2 interface displays a roughly 10 times higher J_{oe} value than the (100) Si-SiO_2 interface following vacuum annealing at 800°C. The (111) Si interface also displays a worse thermal stability than the (100) Si interface. CV measurements show that isothermal and isochronal anneals increase the mid gap defect density and charge density more rapidly for the (111) Si interface than (100) Si interface.

The Si-SiO_2 interface defect density may be influenced by a phosphorus diffusion. However, the observed difference in J_{oe} for the lightly diffused samples studied here is chiefly the result of additional recombination in the diffused region rather than increased recombination at the diffused surface.

The thermal stability of textured and (100) oxidized Si surfaces is compared. Acid etching is applied to the textured surface to form Si surfaces with topologies between textured and (100). The textured surface displays a worse thermal stability than the (100) Si surface, with the thermal stability of the acid etched textured Si surfaces in between these extremes. Longer etching times result in flatter surfaces and a thermal stability closer to the (100) surface.

Chapter 3

LPCVD silicon nitride film properties, and the influence of nitride deposition on the Si-SiO_2 interface

In this chapter the properties of Silicon Nitride films deposited by Low Pressure Chemical Vapor Deposition (LPCVD) are examined. The concentration of bonded hydrogen in the films was measured using Multiple Internal Reflection (MIR), while the positive charge density was

measured using Capacitance Voltage (CV) measurements. The influence of thermal treatments on the nitride film properties is discussed.

$Si_3N_4/SiO_2/Si$ structures are of particular interest for photovoltaic applications. Therefore, the influence of LPCVD nitride deposition on the properties of the $Si-SiO_2$ interface was examined in some detail.

3.1 Introduction

Over the last few years, silicon nitride (SiN_x) deposited by plasma enhanced chemical vapor deposition (PECVD) has become the material of choice as an antireflection coating for silicon solar cells. This can be attributed to the combination of desirable properties that this material possesses: a refractive index that can be tuned to provide an excellent antireflection coating; the ability to achieve very good surface passivation; and the fact that it is possible to considerably improve the bulk of low quality silicon material during high temperature thermal steps following deposition of a PECVD nitride layer. This last property results from the diffusion of hydrogen in the nitride film into the silicon bulk, where it passivates defects [8, 105]

LPCVD silicon nitride, while widely used in the microelectronics field, has not received much attention for photovoltaic applications. In this and the following chapter, the properties of LPCVD nitride films and their influence on the electronic properties of the Si surface are investigated. A schematic of the LPCVD system used to deposit Si_3N_4 in this work is shown in figure 3.1. During deposition in an LPCVD furnace, the wafers are held inside a quartz cage. The reaction is carried out by reacting ammonia (NH_3) and dichlorosilane (SiH_2Cl_2 or DCS) to produce silicon nitride. The reaction is shown in equation 3.1:

$$3SiH_2Cl_2+4NH_3\text{------}Si_3N_4+3Cl_2+6H_2 \qquad (3.1)$$

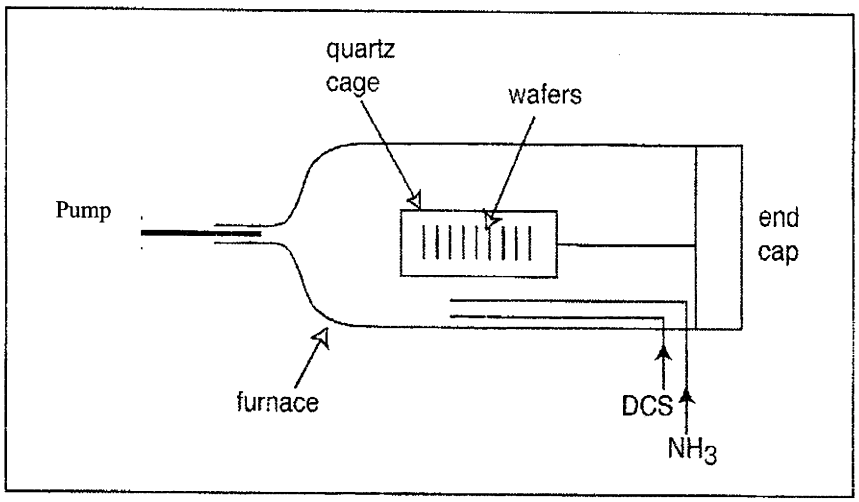

Figure 3.1 A schematic of the LPCVD system used to deposit silicon nitride in this work

There are other reactions occurring in the LPCVD furnace, such as the dissociation of ammonia. Many by-products are formed during the nitride deposition, for example, hydrochloric acid (HCl). This may react with ammonia to form ammonium chloride (NH_4Cl), a white powder that sublimes at 340°C. Ammonium chloride can cause blockage problems in the vacuum system. The HCl, however, can be advantageous as it aids deposition by cleaning both the wafers surface and the deposition equipment.

The deposition process used in this work is described as follows:

- Samples are loaded in furnace and allowed to thermally equilibrate in N_2 for 10 minutes, typically at a temperature of 775°C
- The LPCVD furnace is pumped down to a pressure of 0.5 torr (takes 2 min typically)
- Gases are turned on (typical flow rates: ammonia 120 scc/m (standard-state cubic centimeter per minute) and DCS 30 scc/m) and deposition occurs. The deposition rate is typically 5 nm/min. A deposition of 50 nm nitride normally takes 10 minutes.
- Gases are turned off and the pump evacuates the remaining gases in the furnace(3 mins)
- N_2 gas is turned on to take the chamber up to atmospheric pressure, typically about 5 mins

LPCVD deposited silicon nitride displays very different properties to PECVD SiN_x. If deposition is carried out using an excess of NH_3 (the situation considered in this work), the composition of the nitride is close to stoichiometric and hence may be written as Si_3N_4. When deposited directly on silicon, it provides only very poor surface passivation. Further, the

hydrogen content of LPCVD Si_3N_4 is much lower (2-10 at.%) than that of PECVD SiN_x (20-25 at.%) [4, 5], and LPCVD Si_3N_4 has not been successfully used for the passivation of bulk defects. In fact, it is known that the bulk properties of wafers with LPCVD Si_3N_4 films can degrade substantially and irreversibly if subjected to high temperature processes [106-108].

Despite these disadvantages, LPCVD Si_3N_4 has several properties which make it potentially very useful for silicon solar cells.

-It is an excellent diffusion and oxidation mask[109]. LPCVD Si_3N_4 can be used as more effective diffusion barrier to dopants than oxide. LPCVD Si_3N_4 is relatively impermeable to oxygen and oxidizes very slowly.

- LPCVD Si_3N_4 is hard and scratch resistant[110]. Scratches on the surface can cause shunts in finished solar cells.

-It is resistant to attack by a large range of etchants commonly used for solar cell fabrication, such as alkaline solutions and silicon etchants containing hydrofluoric and nitric acid. LPCVD Si_3N_4 has a much lower etch rate in HF solutions than SiO_2.

- LPCVD Si_3N_4 has a refractive index which is near optimal as an antireflection coating behind glass[110].

-LPCVD Si_3N_4 deposition is highly conformal, such that even obscured surfaces can be coated[111]. This is of particular advantage in novel thin silicon cell structures such as SLIVER cells[13].

-Finally, high volume, batch deposition processes such as low pressure chemical vapor deposition are potentially cheaper than plasma enhanced chemical vapor deposition.

A prerequisite to the use of LPCVD Si_3N_4 as an antireflection coating in high performance solar cells is the ability to achieve excellent surface passivation. In order to take full advantage of its properties, it would be highly desirable to be able to carry out further high temperature steps following nitride deposition, without significantly degrading either the bulk or surface properties of the substrate. It has already been demonstrated that the use of a thin (~25 nm) thermally grown oxide between the wafer and the nitride film allows excellent surface passivation to be achieved[106]. The presence of the oxide will result in only a marginal decrease in the antireflection properties of the optimised oxide/nitride stack. Further, the use of a thin interfacial oxide has also been shown to significantly reduce the degradation of the silicon bulk following further high temperature process steps[106].

3.2 LPCVD Silicon Nitride film properties

3.2.1 Experimental details

A detailed description of MIR and C-V measurements is given in chapter 1. Samples used for MIR measurements were p type, (111), double sided polished, ~500 μm thick. After a standard RCA clean and HF dip to remove the native oxide, around 200 nm LPCVD Si_3N_4 was deposited on both sides of the MIR samples at 775°C and 0.5 torr. The ammonia flow rate was 150 scc/m and the DCS flow rate was 30 scc/m. Selected samples were annealed in nitrogen at 900°C or 1000°C.

FGA was carried out at high temperatures in an attempt to introduce hydrogen back into the nitride film. The MIR wafers were cut into 8 mm×10 mm×0.5 mm pieces. A 45° angle was polished at both edges of each piece before measurements. The sample dimensions result in the light being internally reflected at the Si surfaces about 20 times prior to exiting, thus amplifying the signals due to the H bonds by the same factor. Both bare silicon samples and Si_3N_4 coated samples were measured by MIR, and the spectra from bare Si were subtracted in order to obtain data for the Si_3N_4 layer only.

To determine the charge density and interface properties of LPCVD Si_3N_4 films deposited directly on silicon, Cz, p-type, 10-23 Ωcm, (100) Si samples were used for high frequency (1 MHz) C-V measurements. To ensure a clear comparison, ~100 nm thick LPCVD Si_3N_4 was deposited at 775°C and 0.5 torr. The ammonia flow rate was 120 scc/m and the DCS flow rate was 30 scc/m. About 100 nm thick films of SiO_2 were grown at 1000°C in dry oxygen on selected C-V samples for comparison. One side of the insulator was then removed by HF fuming. About 80 nm of Aluminium was deposited on the insulator (nitride or oxide) with an area of around 4.7×10^{-3} cm^2 through a shadow mask to form metal-insulator-semiconductor (MIS) structures. Ohmic contacts were realized by spreading a thin GaIn layer on the back side of the substrate.

3.2.2 Hydrogen content in LPCVD Si_3N_4 films

Figure 3.2 shows the IR absorbance spectrum from an as deposited sample with a 200 nm thick nitride layer. The N-H and Si-H bond stretching modes give rise to the absorbance peaks at wavenumbers around 3331 cm^{-1} and 2202 cm^{-1}, respectively. It can be seen from the spectrum that the N-H bond concentration is substantially higher than the Si-H bond concentration.

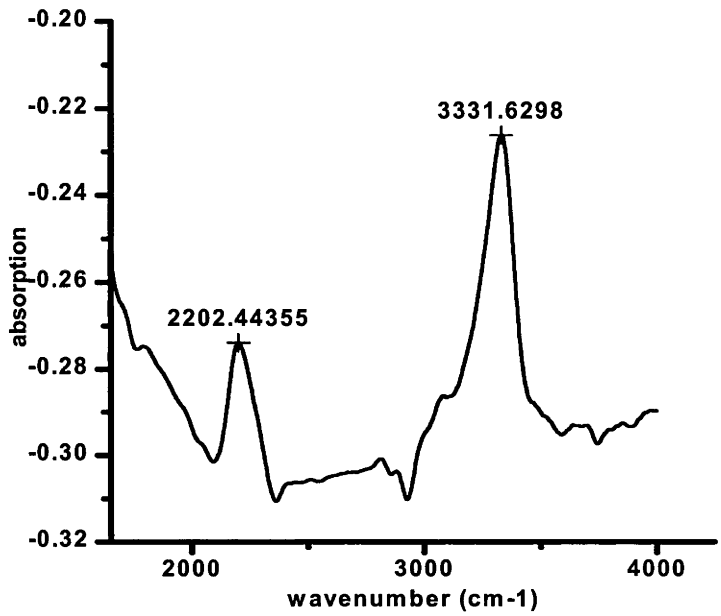

Figure 3.2 absorbance spectrum of 200 nm as deposited LPCVD Si_3N_4 on Si structure.

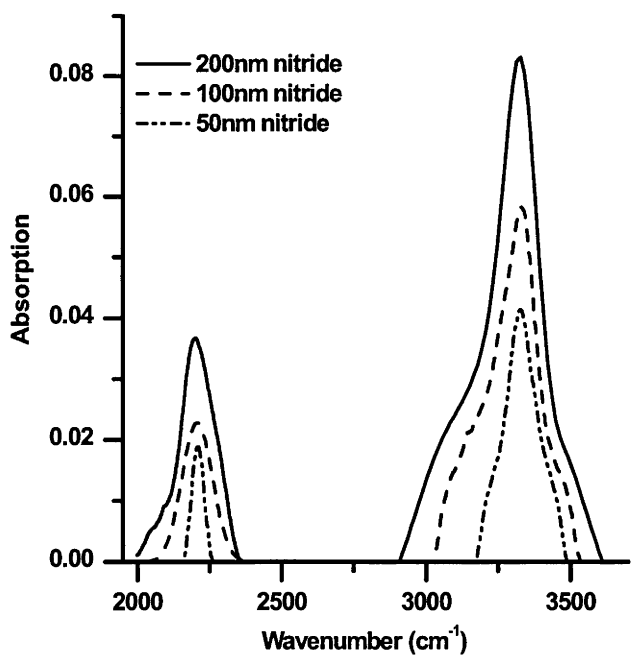

Figure 3.3 Absorbance spectra of 50, 100 and 200 nm thick as deposited LPCVD Si_3N_4 films on Silicon.

A comparison of the spectra from LPCVD Si_3N_4 films with nitride thicknesses of around 200 nm, 100 nm and 50 nm is shown in figure 3.3. All spectra have been baseline corrected and smoothed. For both N-H and Si-H bonds, the integrated areas of N-H and Si-H spectra are directly proportional to the nitride thickness, indicating that the hydrogen concentration in the Si_3N_4 layer is relatively uniformly distributed within the layer. This is in agreement with the results of Figure 3.4, which shows the Secondary Ion Mass Spectroscopy (SIMS) H profile for an LPCVD $Si_3N_4/SiO_2/Si$ structure.

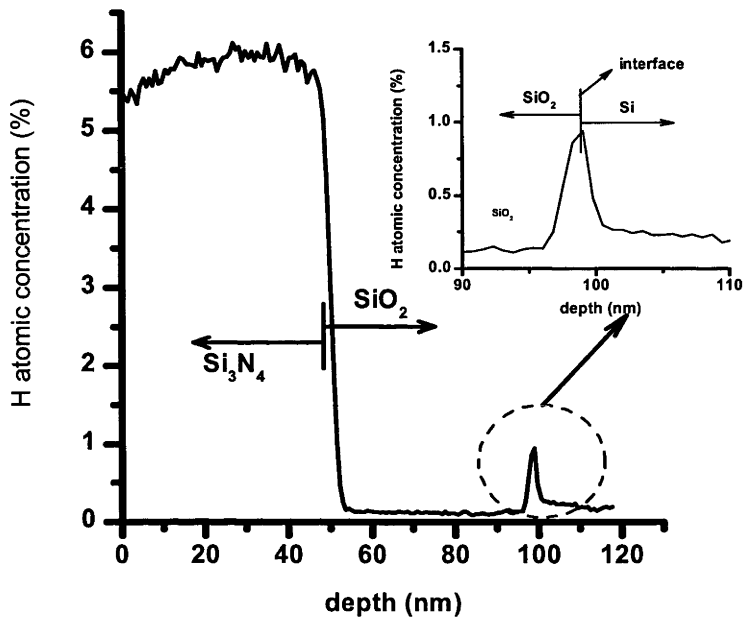

Figure 3.4 SIMS H profile in an LPCVD Si_3N_4/SiO_2 stack on Si. The oxide and nitride layers are both ~50 nm thick. The stack was annealed in N_2 at 400°C for 3 hours following nitride deposition.

3.2.2.1 Effect of thermal anneals on bonded H concentration

A key challenge to the use of LPCVD Si_3N_4 as both a masking material during processing and a final antireflection coating is the ability to maintain good surface passivation at the end of the process. Studies have shown that degradation of surface passivation during high temperature processing is primarily caused by a loss of hydrogen from the Si-SiO_2 interface, where the hydrogen passivates interfacial defects[106-108]. Therefore, studying of the loss of H during thermal annealing is important. In this section, high temperature nitrogen anneals are used to simulate high temperature process steps such as diffusions and oxidations that may be carried out subsequent to nitride deposition in a solar cell process sequence, (as well as the nitride deposition process itself, which is also a relatively high temperature process).

Figure 3.5 shows the FTIR spectra for a 200 nm thick LPCVD Si_3N_4 film on Si after thermal annealing at 900°C and 1000°C in N_2 for 30 minutes. The spectrum for the as deposited nitride film is also shown for comparison. Table 3.1 summarizes the bonded hydrogen concentrations. It is clear that the anneals lead to a breaking of N-H and Si-H bonds in the nitride layer, and a consequent loss of H from the film.

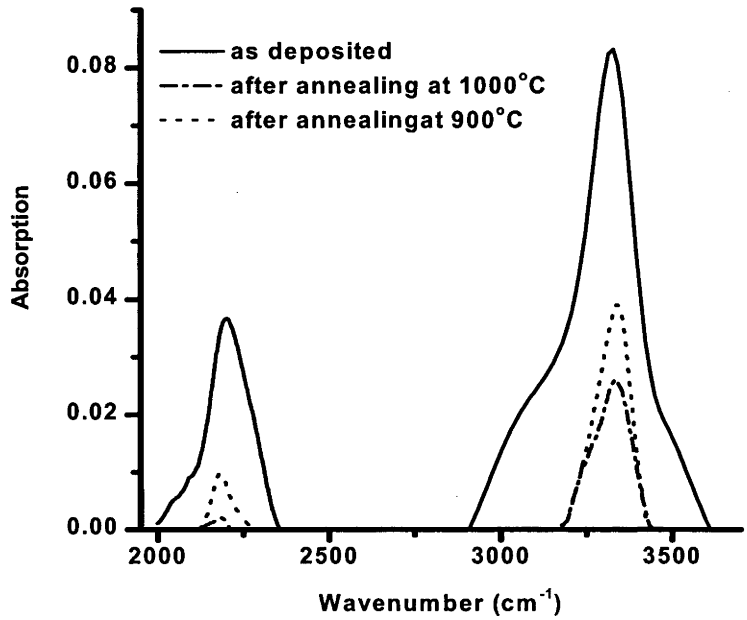

Figure 3.5 Absorbance spectrum of 200 nm LPCVD Si_3N_4 on Si - as deposited and after anneals at 900°C and 1000°C for 30 mins.

	Si-H bond(%)	N-H bond(%)	Total H bond(%)
As deposited	0.8	4.2	5.0
900°C anneal	0.16	0.93	1.1
1000°C anneal	0.014	0.60	0.61

Table 3.1 Comparison of Si-H and N-H bond concentrations is LPCVD Si_3N_4 films following thermal anneals at 900°C and 1000°C for 30 minutes, respectively.

3.2.2.2 H reintroduction by FGA

Hydrogen concentration in the Si_3N_4 following annealing at 900°C

FGA was carried out for one hour at different temperatures following an initial anneal in nitrogen for 30 minutes at 900°C. The absorbance spectra for some of the films measured are shown in figure 3.6. After annealing in nitrogen at 900°C for 30 minutes, both Si-H and N-H

bond concentrations decrease dramatically, while a subsequent FGA significantly increases these concentrations, indicating re-introduction of hydrogen into the nitride film.

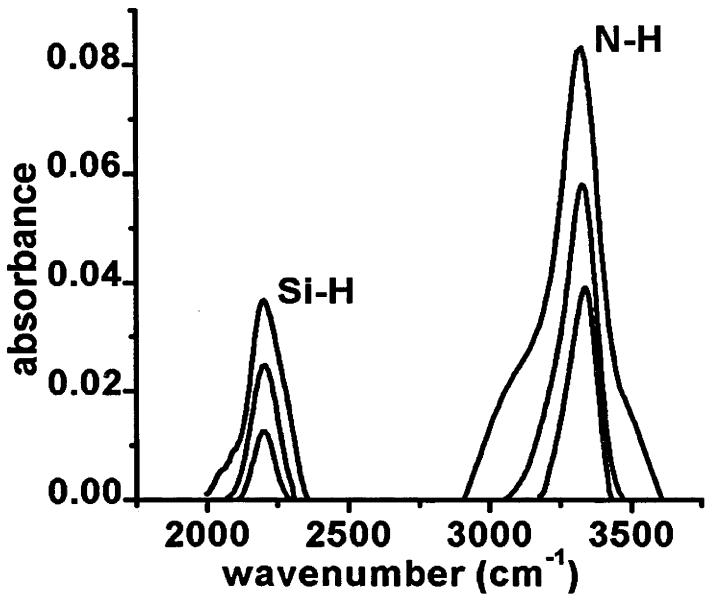

Figure 3.6. Absorbance spectra of the LPCVD nitride films showing N-H bonds (near 3331 cm^{-1}) and Si-H bonds (2202 cm^{-1}). The spectra are, in the order from highest to lowest peaks: as deposited; 30 minute N_2 anneal at 900°C and a subsequent FGA for 1 hour at 840°C, and 30 minute N_2 anneal at 900°C only.

Figure 3.7 summarizes the results of 1 hour isochronal FGAs carried out in the temperature range 800-900°C following a 30 minute nitrogen anneal at 900°C. For reference, the total bonded hydrogen concentration immediately after the N_2 anneal is 1.1%.

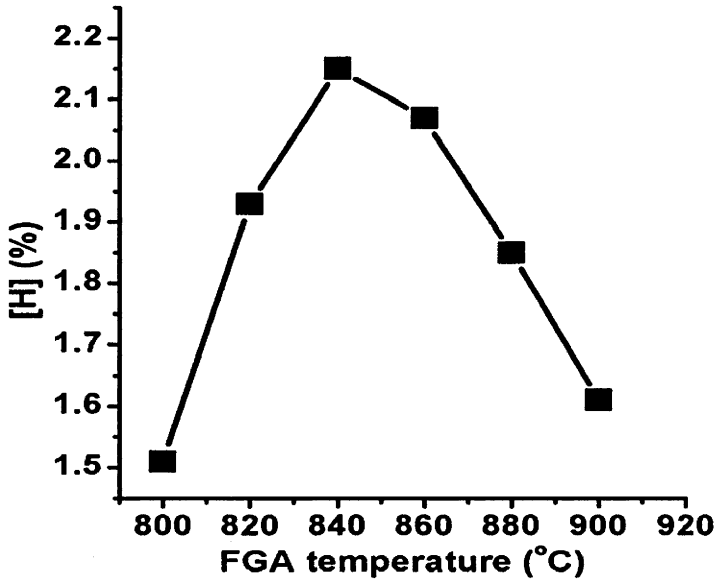

Figure 3.7. Total bonded hydrogen concentrations in the LPCVD Si_3N_4 following a 30 minute N_2 anneal at 900°C and a 1 hour isochronal FGA at temperatures in the range 800-900°C.

It can be seen that for isochronal anneals, there exists an optimum temperature which leads to the greatest density of hydrogen bonds. In the case of the 1 hr anneals performed here, this optimum temperature is close to 840°C. This implies that the equilibrium hydrogen concentration in the nitride film in a forming gas ambient decreases at high temperatures. This finding is consistent with the results of Arnoldbik et al.[94] who inferred from their measurements a decrease in the surface concentration of bonded hydrogen in their nitride films following a 1000°C anneal in 4% H_2, compared to an anneal at 900 or 800°C.

Figure 3.8 shows the results of isothermal FGAs at 840°C on samples that had previously been annealed in nitrogen at 900°C for 30 minutes. The Si-H concentration increases rapidly during the first 30 minutes, after which the increase in concentration is only marginal. In contrast, there is a relatively steady increase in the N-H bond concentration as the anneal time is increased from 0 to 4 hours. The Si-H bond concentration is always much lower than the N-H concentration. As a result, a steady increase in the total bonded hydrogen concentration is observed.

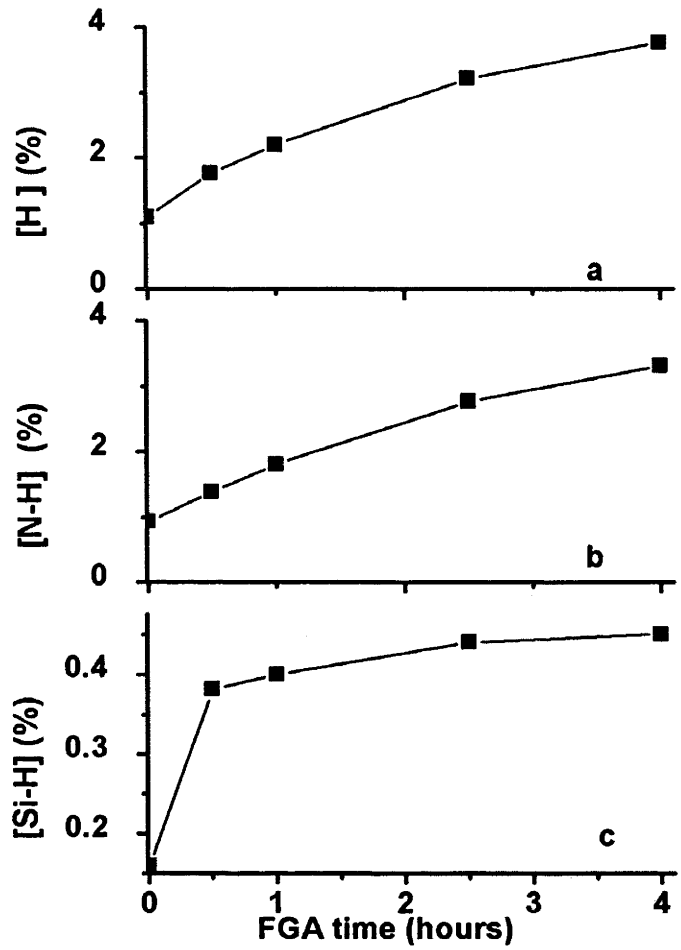

Figure 3.8. Bonded hydrogen concentrations in LPCVD nitride films following a 30 minute N_2 anneal at 900°C and an isothermal FGA at 840°C: a- total hydrogen concentration; b- N-H bond concentration; c- Si-H bond concentration

Hydrogen concentration in Si_3N_4 following annealing at 1000°C

Samples were also annealed at 1000°C in nitrogen for 30 mins, followed by 1 hour isochronal FGAs at various temperatures in the range 800-900°C. Measurements of the bonded hydrogen concentrations again indicated an optimum anneal temperature of around 840°C. In subsequent experiments, therefore, samples were given isothermal FGAs at 840°C after the 1000°C N_2 anneal. Figure 3.9 summarises these results. The higher anneal temperature has resulted in lower initial hydrogen bond concentrations, as well as a somewhat lower rate of re-forming of Si-H and N-H bonds. Compared with Figure 3.8, the hydrogen content for the post 1000°C nitrogen anneal structure following a 4 hour FGA is only around half that of the post 900°C nitrogen

anneal structure. It is clear that the increase in anneal temperature has resulted in a significant change in the properties of the silicon nitride layer.

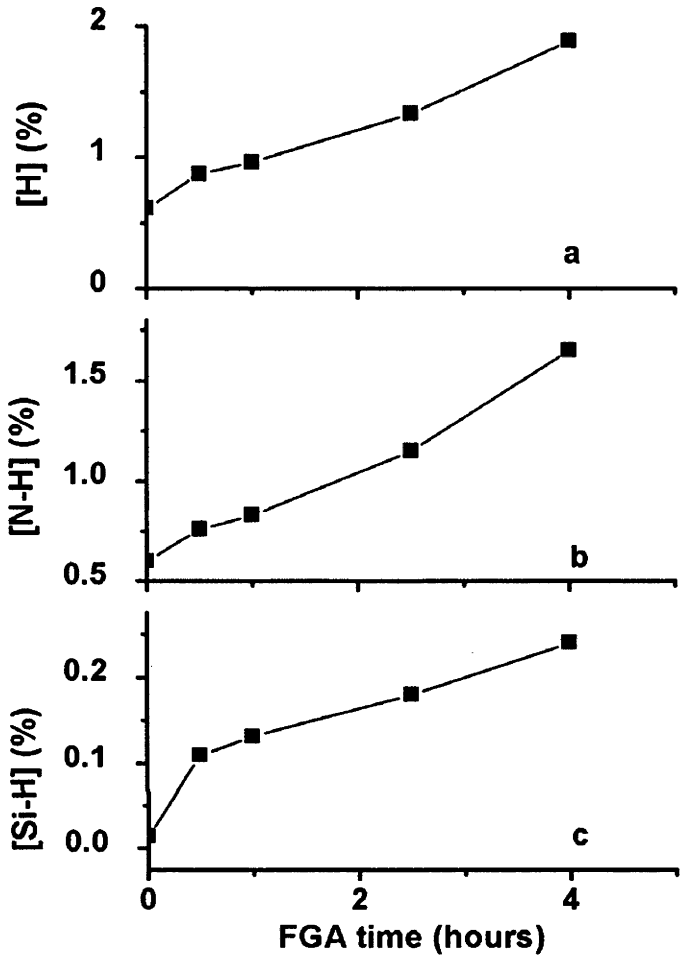

Figure 3.9. Bonded hydrogen concentrations in LPCVD nitride films following a 30 minute N_2 anneal at 1000°C and an isothermal FGA at 840°C: a- total hydrogen concentration; b- N-H bond concentration; c- Si-H bond concentration

The diffusion of hydrogen in LPCVD silicon nitride has been studied by several authors [94, 98, 112-114]. Perhaps the most comprehensive and detailed study is that of Arnoldbik et al.[94] who, using elastic recoil detection (ERD) analysis, determined the diffusion coefficient of hydrogen in LPCVD nitride and oxynitride films over a range of temperatures.

Arnoldbik used similar but not identical nitride film deposition conditions to those used here. The loss of hydrogen from our samples is substantially more rapid than that observed by Arnoldbik et al.[94], who found a decrease in the total amount of bonded hydrogen to about 30% of its initial value after a 30 min, 1000°C anneal, for nitride films of similar thickness to those used here. In contrast, we find a reduction to 10% of the initial concentration for the same anneal

conditions. The difference may be a result of the different deposition conditions, such as the slightly lower deposition temperature used here (775°C compared to 800°C). Arnoldbik et al. explained the process of hydrogen reintroduction into Si_3N_4 films annealed in molecular hydrogen at high temperatures as a two-step reaction. In the first step, molecular hydrogen diffuses into a surface layer of Si_3N_4 to form N–H and Si–H bonds. The subsequent step is the diffusion of the bonded hydrogen from the surface deeper into the film, with this step requiring first the breaking of hydrogen bonds and then the diffusion of atomic hydrogen into the film. It is likely that the same mechanism is responsible for the observations reported here.

3.2.3 Charge in LPCVD Si_3N_4 films

3.2.3.1 Charge in the as deposited Si_3N_4 film

Figure 3.10 shows the HFCV curves for metal-LPCVD Si_3N_4-Si and metal-SiO_2-Si structures. The flat band shifts (relative to an ideal MIS structure with Al gate and no insulator charge) for the nitride and oxide samples are -8.1 V and -1.25 V, respectively. The calculated values for the effective net interface charge densities are 3.1×10^{12} and 2.5×10^{11} cm^{-2}, respectively.

The large amount of positive charge in the nitride films may result from interface defects, or from the type of bulk defect known as a K centres[115]. The effect of charge in LPCVD nitride films has also been discussed by other authors[116], who presented evidence that the charge is distributed at least through the first 15 nm of their nitride films.

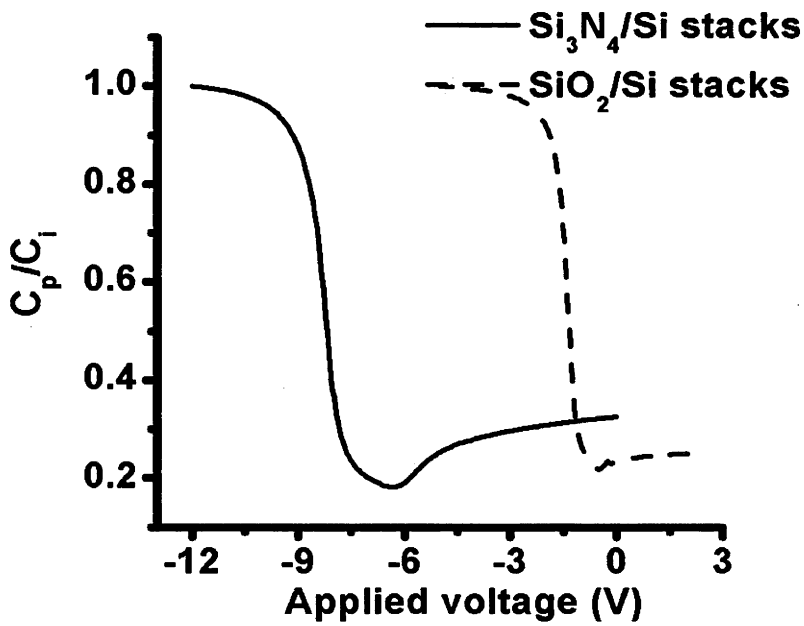

Figure 3.10. High Frequency C-V curves for ~100 nm LPCVD nitride and thermally grown oxide layers on silicon. The sweep is from inversion to accumulation.

3.2.3.2 Hysteresis effect

Figure 3.11 shows the hysteresis effect observed on HFCV curves of LPCVD Si_3N_4/Si stacks just after deposition. The flat band voltage is -8.1 V when sweeping the voltage from accumulation to inversion and -9.2 V sweeping from inversion to accumulation, giving values for the effective charge density of $+3.1\times10^{12}$ cm^{-2} and $+3.5\times10^{12}$ cm^{-2}.

This type of behaviour is also observed in PECVD SiN_x films[6] where it has been attributed to the charging and discharging of interface traps due to the tunnelling of holes from the Si surface to interface defect sites. The same mechanism is likely to be operative here.

Table 3.2 summarizes the flat band and hysteresis voltages, and charge densities for various samples. For these measurements, 100 nm Si_3N_4 layers were deposited on p type Si substrates with a DCS flow rate of 30 scc/m and ammonia flow rates of 120,150,180 and 210 scc/m, respectively. All depositions were done at 775°C and 0.5 torr. With an increase in deposition gas flow ratio, the effective charge density and hysteresis voltage decrease. Thus, with increasing NH_3/DCS flow ratio, there appears to be a decrease in the density of interface traps which can be charged and discharged as a result of applying a varying bias voltage.

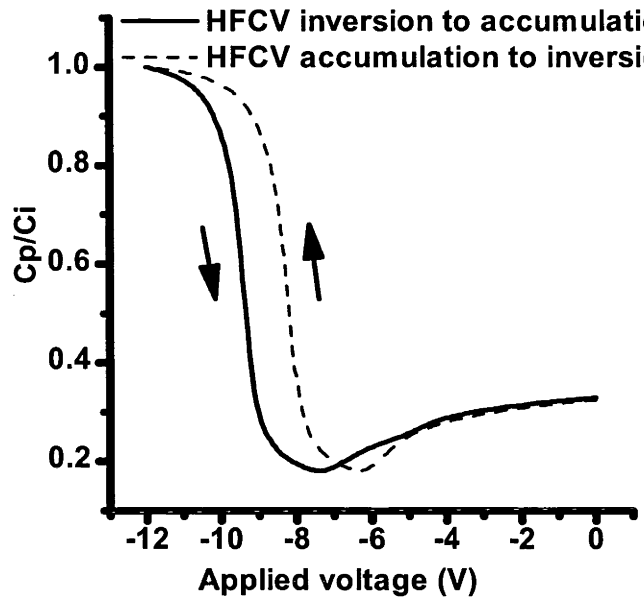

Figure 3.11. HFCV curves for a 100 nm Si_3N_4 film on Si. The dashed line represents sweeping from accumulation to inversion and the solid line represents sweeping from inversion to accumulation.

NH_3 to DCS ratio	V_{fb1} (V)	Q_1 (10^{12} cm^{-2})	V_{fb2} (V)	Q_2 (10^{12} cm^{-2})	ΔV (V)	ΔQ (10^{12} cm^{-2})
4	-8.1	3.10	-9.2	3.5	-1.1	0.42
5	-7.6	2.91	-8.2	3.14	-0.6	0.23
6	-7.4	2.83	-7.9	3.02	-0.5	0.19
7	-7.3	2.79	-7.7	2.95	-0.4	0.15

Table 3.2. LPCVD Si_3N_4 deposition ratio dependence of flat band voltage V_{fb1} (sweeping from inversion to accumulation) and the corresponding charge density Q_1, flat band V_{fb2} (sweeping from accumulation to inversion) and the corresponding charge density Q_2, and flat band difference ΔV ($\Delta V = (V_{fb2} - V_{fb1})$ due to hysteresis and the corresponding charge density ΔQ.

3.2.3.3 High frequency CV measurements of LPCVD Si_3N_4 on SiO_2/Si

Figure 3.12 shows the HFCV curves for Si_3N_4/Si and $Si_3N_4/SiO_2/Si$ structures. The nitride is 50 nm thick for both structures and the oxide is 50 nm thick. Each structure was swept from accumulation to inversion and from inversion to accumulation. Figure 3.13 shows the oxide thickness dependent charge density for $Si_3N_4/SiO_2/Si$ stacks. The nitride is 50 nm thick. The sweep direction is from inversion to accumulation. With no oxide (at zero oxide thickness), the effective charge density is about 3.5×10^{12} $/cm^2$. Even a very thin oxide greatly reduces the

charge density to about 1.1×10^{12} /cm^2. The reduction of charge in the nitride by inserting an oxide layer suggests that the majority of charge in the nitride layer of Si_3N_4/Si structures is due to defects at the Si-Si_3N_4 interface. When an oxide layer is introduced, the defect density at the Si surface is greatly reduced. The density of charged defects at the SiO_2-Si_3N_4 interface appears to be much lower than that at the Si-Si_3N_4 interface.

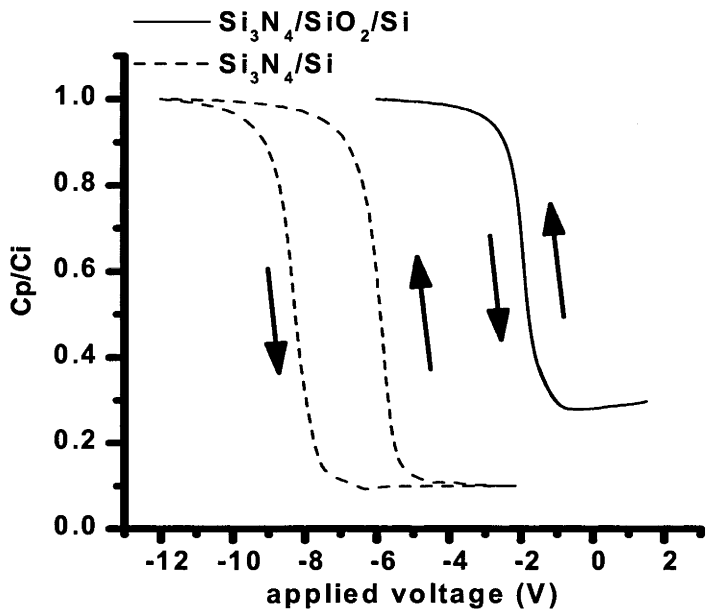

Figure 3.12. High frequency C-V curves for Si_3N_4/Si structure and $Si_3N_4/SiO_2/Si$ structures. The nitride is 50 nm thick for both structures and the oxide is 50 nm thick. Cp is the measured capacitance and Ci is the insulator capacitance

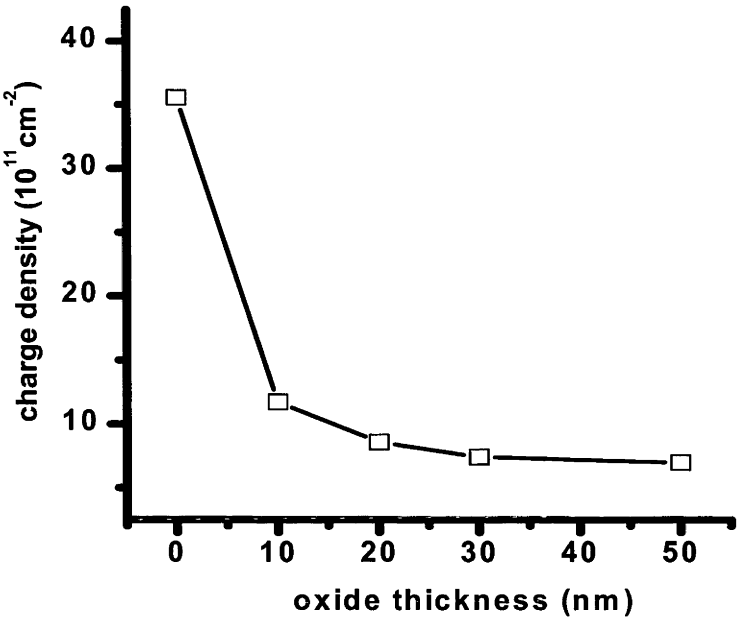

Figure 3.13. Oxide thickness dependent charge density for $Si_3N_4/SiO_2/Si$ stacks. The nitride thickness is 50 nm.

Hysteresis was also observed for 50 nm Si_3N_4/Si structures. As shown in figure 3.12, the flatband voltage is –6.1 V and –8.7 V sweeping from inversion to accumulation and from accumulation to inversion, respectively. However, no hysteresis was observed for $Si_3N_4/SiO_2/Si$ structures.

3.2.3.4 Effect of thermal annealing on charge density

Thermal annealing in N_2 of LPCVD nitride layers above the nitride deposition temperature has been shown to result in the removal of hydrogen from the nitride layer, through the breaking of Si-H and N-H bonds and the subsequent out-diffusion of hydrogen. High temperature anneals in forming gas re-introduce hydrogen into the Si_3N_4 film. Figure 3.14 shows the high frequency C-V curves measured after thermal annealing at 900°C and 1000°C for 30 minutes on p type metal-nitride-Si structures. The nitride layers were 100 nm thick.

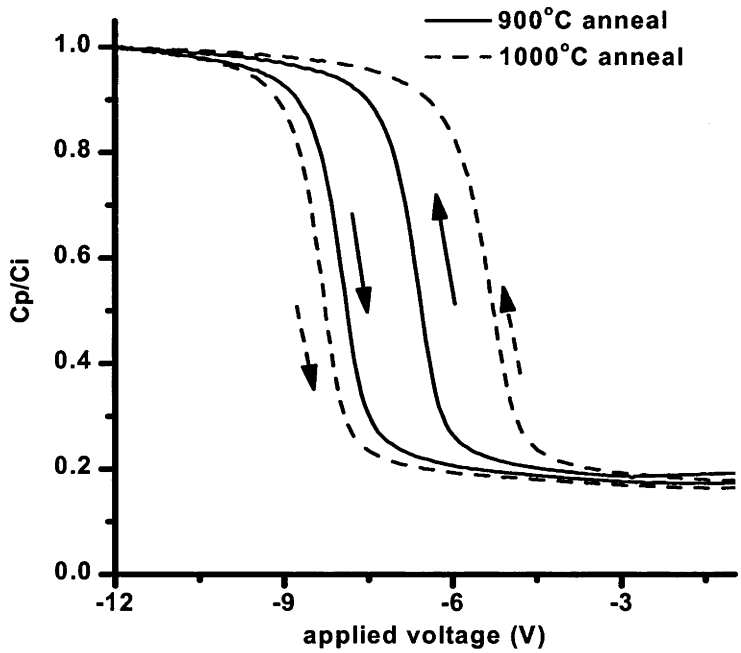

Figure 3.14. High frequency C-V curves for p type Metal-Nitride-Si structures after 30 minute annealing in N_2 at 900°C and 1000°C, respectively. The nitride is 100 nm thick.

The HFCV curves for p type metal-nitride-Si structures measured after thermal annealing in N_2 at 900°C or 1000°C, and a subsequent anneal in forming gas at 840°C for 30 minutes, are shown in figure 3.15. Table 3.3 summarizes the flat band voltages and corresponding charge densities measured after annealing in N_2 at 900°C and 1000°C for 30 minutes, and after subsequent FGAs at 840°C for 4 hours.

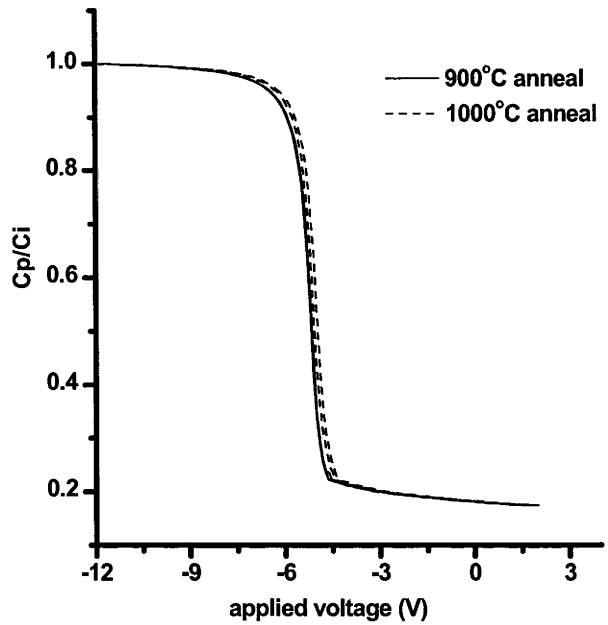

Figure 3.15. High frequency C-V curves for p type Metal-Nitride-Si structures after 30 minute annealing in N_2 at 900°C and 1000°C and a subsequent annealing in forming gas at 840°C. The nitride is 100 nm thick.

	V_{fb1} (V)	Q_1 (10^{12} cm^{-2})	V_{fb2} (V)	Q_2 (10^{12} cm^{-2})	ΔV (V)	ΔQ (10^{12} cm^{-2})
As deposited	-8.1	3.10	-9.2	3.5	-1.1	0.42
900°C anneal	-6.6	2.54	-8	3.1	-1.33	0.51
1000°C anneal	-5.6	2.14	-8.2	3.14	-2.6	1.0
900°C anneal+FGA	-5.02	1.92	-5.04	1.93	-0.02	0.01
1000°C anneal+FGA	-5.19	1.98	-5.21	1.99	-0.02	0.01

Table 3.3. Thermal anneals in N_2 and in forming gas on LPCVD Si_3N_4/Si structures. Influence on flat band voltage V_{fb1} (sweeping from inversion to accumulation) and the corresponding charge density Q_1, flat band V_{fb2} (sweeping from accumulation to inversion) and the corresponding charge density Q_2, and flat band difference ΔV ($\Delta V = (V_{fb2} - V_{fb1})$ due to hysteresis and the corresponding charge density ΔQ.

The increase in hysteresis following high temperature processing indicates an increase in the density of defects near the Si-Si_3N_4 interface which can be charged and discharged via the tunneling of holes from the Si surface.

The change in charge density as a result of thermal treatments could result from changes in the nitride bulk. During high temperature processes, hydrogen is driven away from the nitride film, leaving behind dissociated Si and N bonds which may rearrange into Si-Si, Si-N and N-N bonds, thereby effectively eliminating defects from the film. The decrease in charge density after HTAs is therefore the result of bulk defect removal in the nitride film. The location of the charge cannot be determined from the measurements presented here; it may be uniformly or non-uniformly distributed throughout the nitride layer; or it may reside chiefly near the interface (but sufficiently removed from the interface that tunnelling of carriers between the defects and the Si bulk does not occur). N_2 annealing leads to densification of the film and the removal of defect sites (see results of sections 3.2.2.2, 3.2.3 and 4.4.2.2)

A high temperature FGA introduces hydrogen into the nitride bulk where it passivates defects by forming Si-H and N-H bonds. The virtual elimination of hysteresis indicates effective passivation of these near-interface defects. However, the high temperature FGAs result in only a modest reduction in the bulk charge density.

3.2.4 LPCVD Si_3N_4 film density

Qualitative information on the LPCVD Si_3N_4 film density was obtained by measuring the etch rate in buffered HF solution (10% HF in 90% NH_4F). A lower nitride layer density is generally correlated with a higher etching rate[117].

Annealing at a high temperature has the effect of densifying the LPCVD nitride film, indicated by a decrease in the buffered HF etch rate after anneals. Table 3.4 shows the etch rates for nitride on silicon following deposition (with an ammonia to DCS flow rate of 4:1, at 775°C and 0.5 torr) and after subsequent HTAs at 900°C and 1000°C for 30 minutes.

process	Etching rate (nm/min)
As deposited	0.94
900°C annealing	0.72
1000°C annealing	0.65

Table 3.4. LPCVD Si_3N_4 film etch rate

A slower etching rate indicates a denser LPCVD nitride film[117]. During HTAs, hydrogen is driven away from the nitride film, leaving behind dissociated Si and N bonds which may rearrange into Si-Si, Si-N and N-N bonds, thereby effectively eliminating defects from the film.

The change of charge density after HTAs is likely to be the result of the same process of defect removal, since charged bulk defects within the nitride are responsible for a fraction of the measured charge. A post nitrogen anneal in forming gas at 840°C for 4 hours has nearly no influence on the etching rate, indicating the film density depends on the thermal budget but is not influenced much by hydrogen reintroduction.

3.3 Si surface properties in Nitride/Oxide/Si stacks

Compared to PECVD nitride, direct deposition of LPCVD Si_3N_4 on Si does not provide good Si surface passivation. LPCVD nitride deposition usually occurs at 750–800°C, resulting in a relatively low hydrogen concentration[4, 5] (2 to 10%) in the nitride film compared to PECVD SiNx films (20 to 25%). Previous work[106-108] has shown that a thin SiO_2 layer should be grown before Si_3N_4 deposition to prevent irreversible bulk damage caused by stress from the nitride layer. Such LPCVD $Si_3N_4/SiO_2/Si$ stacks can act as effective antireflection coatings and simultaneously allow good surface passivation to be achieved.

In this section, the influence of LPCVD Si_3N_4 film deposition on the Si surface properties is discussed. The Si interface properties of Si_3N_4/Si and $Si_3N_4/SiO_2/Si$ stacks are compared. An important discovery is that LPCVD Si_3N_4 deposition on SiO_2/Si stacks changes the concentration of interface defects. The influence of LPCVD Si_3N_4 deposition conditions, charge in nitride layer, nitride thickness and oxide thickness on Si surface properties is investigated. Hydrogen reintroduction in to the Si-SiO_2 interface by FGA at high temperature is studied. The thermal stability of the Si-SiO_2 interfaces from nitride coated and removed stacks is also investigated.

3.3.1 Interface electronic properties of LPCVD Si_3N_4/Si stacks.

3.3.1.1 Experimental details

For lifetime measurements, (111), n/P, ~100 Ωcm, 500 μm thick Si wafers were used as the starting material. Cz, (100), ~500 μm thick wafers were used as the starting material for C-V measurements. The resistivity was 10-23 Ω-cm for p type wafers and 3-10Ω-cm for n type wafers. The processing details of C-V and lifetime samples are listed in tables 3.5 and 3.6, respectively.

Step	Description	Chemical	Details
1	Saw damage etch	$HF:HNO_3$ solution (1:10)	Remove saw damage from Si surface and edges by etching in $HF:HNO_3$ solution for 3 minutes.
2	RCA 1clean	5:1:1 $H_2O:NH_4OH:H_2O_2$ solution	For 10 minutes in warm solution (~80°C)
3	RCA 2 clean	5:1:1 $H_2O:HCl:H_2O_2$ solution	For 10 minutes in warm solution (~80°C)
4	HF dip	Clean 10% HF solution	Until hydrophobic to remove native oxide
5	LPCVD deposition	Ammonia (120 scc/m) and DCS (30 scc/m)	775°C and 0.5 torr for 20 minutes to deposit ~100 nm Si_3N_4
6	FGA	Forming gas	400°C for 30 minutes
7	High Temperature Anneal (HTA)	N_2	900°C and 1000°C for 30 minutes on selected samples
8	'Rear' nitride removal	HF	Nitride was removed from one side by HF fuming
9	Al deposition	Al	At high vacuum ($<3\times10^{6}$torr), ~80 nm thick Al was deposited on oxide layer through a shadow mask with area of 4.7×10^{-3} cm^2
10	Ohmic contact	Ga-In	Ohmic contact by Ga-In paste on nitride free Si side.

Table 3.5 experimental processes for C-V sample preparation

Step	Description	Chemical	Details
1	Quartering	---	Wafers were cut by a diamond saw into quarters and labelled
2	Saw damage etch	$HF:HNO_3$ solution (1:10)	Remove saw damage from Si surface and edges by etching in $HF:HNO_3$ solution for 3 minutes.
3	HF dip	10% HF solution	Until hydrophobic to remove native oxide
4	RCA 1 clean	5:1:1 $H_2O:NH_4OH:H_2O_2$ solution	For 10 minutes in warm solution (~80°C)
5	RCA 2 clean	5:1:1 $H_2O:HCl:H_2O_2$ solution	For 10 minutes in warm solution (~80°C)
6	HF dip	Clean 10% HF solution	Until hydrophobic to remove native oxide
7	Oxidation	Oxygen	1000°C in dry oxygen for 40 minutes to grow ~50 nm oxide on selected samples, followed by insitu anneal in N_2
8	FGA	Forming gas	400°C for 30 minutes
9	LPCVD deposition	Ammonia (120 scc/m) and DCS (30 scc/m)	775°C and 0.5 torr for 10 minutes to deposit ~50 nm Si_3N_4
10	High Temperature Anneal (HTA)	N_2	900°C for 30 minutes
11	Nitride removal	Phosphoric acid solution	Hot Phosphoric acid solution (~170°C) to remove nitride without

			etching oxide or Si.
12	Re-oxidation	O_2	1000°C in dry oxygen for 40 minutes
13	FGA	Forming gas	400°C for 30 minutes

Table 3.6 experimental processes for LIFETIME sample preparation

3.3.1.2 Lifetime evidence of (111) Si bulk damage caused by LPCVD Si_3N_4 deposition and thermal annealing

Figure 3.16 shows the influence of direct deposition of LPCVD Si_3N_4 on Si bulk lifetime.

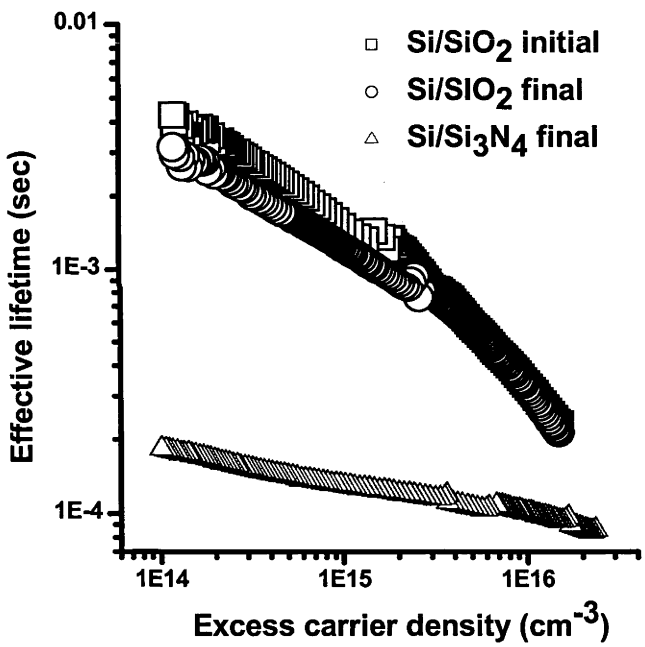

Figure 3.16. Effective lifetime for (111) Si/SiO_2

The curve labelled 'Si/SiO_2 initial' represents the lifetime of a wafer with 50 nm oxide after FGA at 400°C just before LPCVD nitride deposition. The 'Si/SiO_2 final' curve represents the same wafer after a LPCVD Si_3N_4 deposition, HTA at 900°C for 30 minutes, nitride removal and FGA. For comparison, 50 nm LPCVD nitride was deposited on a bare Si wafer. The nitride/Si structure was HTAed at 900°C for 30 minutes. The nitride was removed followed by growth of a 50 nm oxide at 1000°C and a FGA. Lifetime was measured and labelled 'Si/Si_3N_4 final'.

The oxide between the Si_3N_4 layer and the (111) surface acts as a lifetime protection layer, which is consistent with previous results on (100) surfaces[106]. Without the oxide layer, Si bulk damage occurs during LPCVD deposition and subsequent thermal annealing, indicated by the low effective lifetime. Note that the poor effective lifetimes can positively be attributed to bulk damage since the Si surfaces were well passivated by a high quality, FGAed oxide (The damage is not at or near the surface. The sample was etched in $HF:HNO_3$ solution to strip ~20 μm Si. After an ~50 nm oxidation and FGA, the lifetime is still very low) . A slight decrease in effective lifetime is observed for the Si/SiO_2 final curve compared with the initial one, which will be discussed in the following sections.

3.3.1.3 C-V determination of Si_3N_4-Si interface defects

C-V curves and interface defect distribution curves for the $Si\text{-}Si_3N_4$ interface after LPCVD nitride deposition, and after subsequent annealing at 900°C and 1000°C, are displayed in figures 3.17 and 3.18. The nitride thickness is about 100 nm. The interface defect density within the Si forbidden gap for the as deposited Si/Si_3N_4 stacks is much higher than the defect density at a well passivated Si interface, as will be shown later. It can be seen that high temperature anneals change the shape of the defect distribution, as well as dramatically increasing the interface defect density.

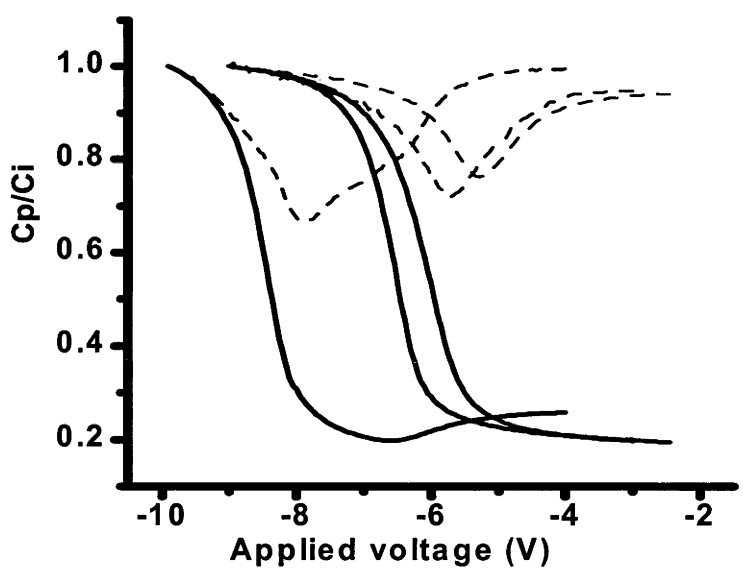

Figure 3.17. C-V curves from p type Si for as deposited Si_3N_4/Si stacks (black lines), Si_3N_4/Si stacks after 900°C anneal (red lines) and Si_3N_4/Si stacks after 1000°C anneal (blue lines). The solid curves represent HFCV curves. The dashed curves represent QSCV curves.

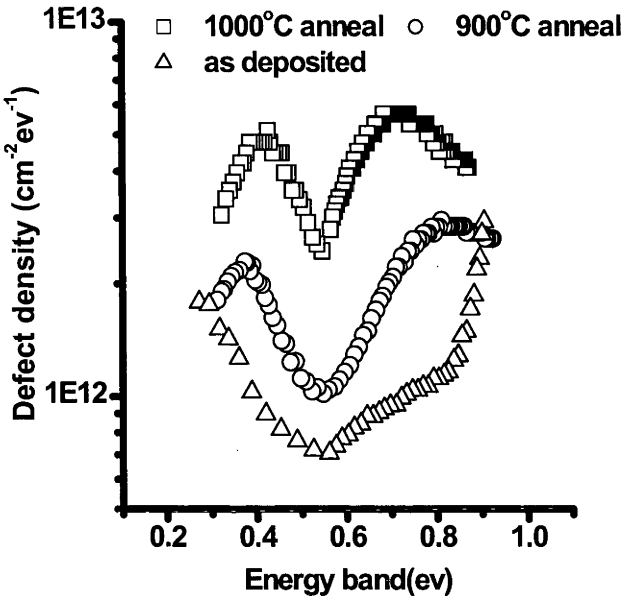

Figure 3.18. Si-Si_3N_4 interface defect distribution within the Si forbidden band gap after 100 nm thick Si_3N_4 deposition and annealing in N_2 at 900°C and 1000°C for 30 minutes.

Table 3.7 shows the mid gap D_{it} values for Si_3N_4/Si stacks and $Si_3N_4/SiO_2/Si$ stacks after HTAs at 900°C and 1000°C for 30 minutes. The oxide and nitride thickness are about 100 nm. The Si_3N_4 layers were removed from the $Si_3N_4/SiO_2/Si$ stacks, followed by an FGA at 400°C for 30 minutes just before the C-V measurements. Just after annealing at 900°C and the removal of the LPCVD nitride (before FGA), the mid gap D_{it} is 6.4×10^{10} $cm^{-2}eV^{-1}$ for the $Si_3N_4/SiO_2/Si$ stacks. Once again, the presence of an oxide layer between the nitride and Si improve the Si interface properties by reducing interface defect density during HTAs. Similar results are observed for thinner oxides as well. For example, table 3.8 shows J_{oe} values for $Si_3N_4/SiO_2/Si$ stacks with a 25 nm thick oxide. The mid-gap Dit for $Si_3N_4/SiO_2/Si$ samples after annealing at 900°C is consistent with the values reported by Xu and Kapoor[118].

	Si_3N_4/Si stacks Mid gap D_{it} ($\times10^{10}$ $eV^{-1}cm^{-2}$)	Nitride removed SiO_2/Si no FGA Mid gap D_{it} ($\times10^{10}$ $eV^{-1}cm^{-2}$)	Nitride removed SiO_2/Si after FGA Mid gap D_{it} ($\times10^{10}$ $eV^{-1}cm^{-2}$)
As deposited	72	--	4.2
900°C annealing	110	6.4	4.2
1000°C annealing	240	--	4.3

Table 3.7. Mid gap D_{it} of Si_3N_4/Si stacks and $Si_3N_4/SiO_2/Si$ stacks after HTA at 900°C and 1000°C. Nitride layer was removed for the $Si_3N_4/SiO_2/Si$ stacks and a FGA was conducted just before C-V measurements. One $Si_3N_4/SiO_2/Si$ stacks received annealing at 900°C and nitride removal but no FGA.

	J_{oe} (fA/cm^2/side)
As deposited	23
900°C anneal	25
1000°C anneal	26

Table 3.8. J_{oe} of Si_3N_4/Si stacks and $Si_3N_4/SiO_2/Si$ stacks after HTA at 900°C and 1000°C. Nitride layer was removed for the $Si_3N_4/SiO_2/Si$ stacks and a FGA was conducted just before J_{oe} measurements.

3.3.2 Defect generation at the Si-SiO_2 interface during LPCVD Si_3N_4 deposition

In this section, the Si-SiO_2 interface defect properties and density after LPCVD nitride deposition are examined by EPR, C-V and lifetime measurements. The Si surface recombination velocity is determined by lifetime and lifetime-voltage measurements. Elemental analysis was carried out by SIMS. The thermal stability of the as oxidized SiO_2/Si stacks and LPCVD nitride removed SiO_2/Si is compared.

3.3.2.1 Experimental details

Samples used for EPR measurements were p-type, ~10 Ω-cm, (111) Cz silicon wafers. Samples were cut with a diamond saw into 25 mm×2.5 mm pieces. They were subsequently etched to remove saw damage from the surfaces. After a standard RCA clean, an oxide layer around 50 nm thick was thermally grown on both sides at 1000°C (samples A, B, C). LPCVD Si_3N_4 deposition was done at 775°C and 0.5 torr, with an ammonia to DCS flow ratio of 4:1, giving ~50 nm stoichiometric nitride layers on both sides of selected wafers (samples B and C). To prevent interference with the Si-SiO_2 interface signal from K centers in the nitride layer[115], the nitride layers for samples B and C were removed in hot phosphoric acid solution without significantly etching the oxide layer. Some of the wafers on which the nitride layer had been removed were oxidized again for 30 min at 1000°C (samples C). On all EPR samples, an RTA was carried out at 800°C for 3 minutes in a high flow of nitrogen gas to de-passivate the Si-SiO_2 interface. A standard RCA clean and DI water rinse were carried out before EPR measurement.

Samples for SIMS measurements are single side polished, p type, (100), 10-23 Ωcm. After a standard RCA cleaning and HF dip, ~50 nm oxide was thermally grown at 1000°C in dry oxygen. ~50 nm LPCVD nitride was subsequently deposited on both sides of the samples. N was profiled in Si_3N_4 and SiO_2 films.

Cz, (100), ~500 μm thick wafers were used as the starting materials for C-V measurements. The resistivity was 10-23 Ω-cm for p type wafers and 3-10 Ω-cm for n type wafers. After a standard RCA cleaning, about 100 nm oxide layer was grown with an insitu anneal in N_2 on p and n type Si samples and about 50 nm nitride layer was deposited on selected samples at 775°C and 0.5 torr with ammonia to DCS ratio of 4:1. The nitride was then removed from the samples in hot phosphorous acid solution, followed by an FGA at 400°C for 30 minutes. Some nitride removed samples received a RTA. One side of the insulator was carefully removed by HF fume and ~80 nm Al was deposited through a shadow mask with an area of 4.7×10^{-3} cm^{-2}. Ohmic contact was achieved by GaIn pasted applied to the Si bulk.

For lifetime measurements, (100), p/B, ~100 Ωcm, 500 μm, Si was used as the starting materials. After a standard RCA cleaning, the samples were lightly phosphorus diffused (R_{sh}=300-400 Ω/□) and about 50 nm oxide layer was grown with an insitu anneal in N_2 on Si samples and about 50 nm nitride layer was deposited on selected samples at 775°C and 0.5 torr with ammonia to DCS ratio of 4:1. The nitride was then removed from the samples in hot phosphoric acid solution, followed by an FGA at 400°C for 30 minutes. Some samples received a RTA before measurements.

To check if immersion of samples in hot (~175°C) phosphoric acid solution (used to selectively remove the LPCVD nitride layer) affects the $Si-SiO_2$ interface properties, some Si samples with thermally grown oxides were immersed in hot phosphoric acid solution together with the nitride samples. Lifetime measurements showed no significant degradation of J_{oe}. Therefore, it was concluded that etching in hot phosphoric acid solution has little effect on $Si-SiO_2$ interface defect properties.

3.3.2.2 Observation of new defect at the $Si-SiO_2$ interface of LPCVD $Si_3N_4/SiO_2/Si$ stacks

Figure 3.19 displays EPR signals from samples A and B. Table 3.9 shows a more detailed comparison between the standard P_b signal from the $Si-SiO_2$ interface (sample A), the signal from sample B (following nitride deposition and subsequent removal) and re-oxidized sample C. The g// value from sample B is smaller than the standard P_b value (sample A).

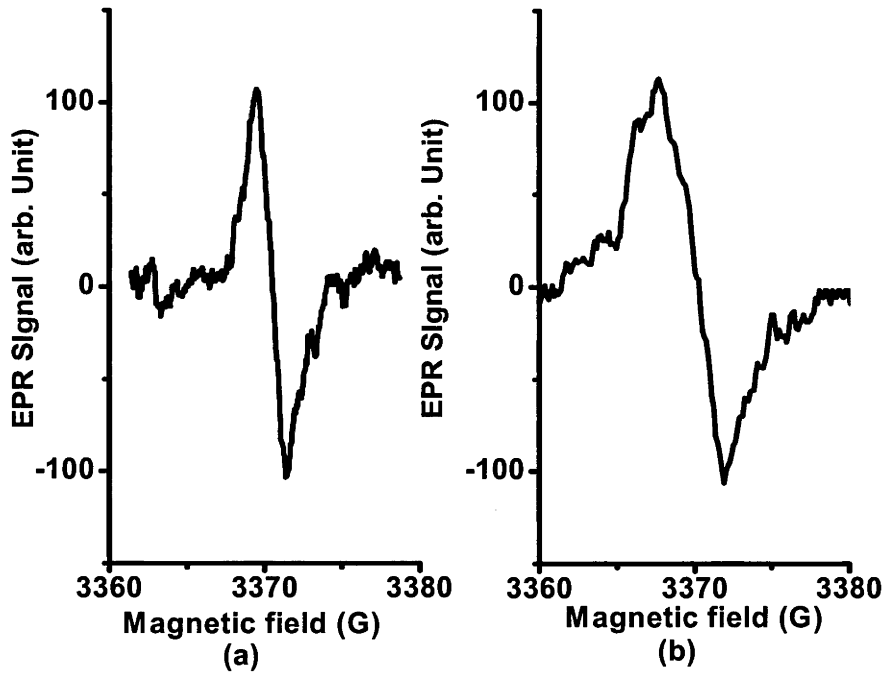

Figure 3.19. EPR signals for (a) samples A (as oxidised) and (b) samples B (following nitride deposition and removal) with the magnetic field set parallel to (111) direction.

For sample B, the P_b like character of the defect is evidenced by the variation of the g value as a function of angle of the magnetic field relative to the (111) direction g(θ), which is well fitted by the equation:

$$g(\theta)=[(g//\cos(\theta))^2+(g\perp\sin(\theta))^2]^{1/2} \qquad (4.1)$$

where θ is the angle between (111) direction and magnetic field direction[119]. The dependence of the g values with θ is shown in figure 3.20. All measured data are well fitted by equation 4.1.

	A as oxidised	B nitride dep. and removal	C re-oxidised
g//	2.00141	2.00125	2.00135
ΔBpp// (G)	1.9	4.1	3.6
g⊥	2.00860	2.00862	2.00858
ΔBpp⊥ (G)	3.8	5.1	4.5
$[P_b]$ (10^{13} cm^{-2})	0.8	1.9	1.0

Table 3.9. Comparison of the g value, peak to peak linewidth (ΔB_{pp}) and paramagnetic defect concentration of samples A, B, C. '//' indicates magnetic field parallel to (111) direction, '⊥' indicates magnetic field perpendicular to (111) direction. The error in the g value is 4×10^{-5}.

Re-oxidation (sample C) has the effect of increasing the g// value. The g⊥ values for all samples are the same within the limits of experimental error. The ΔB_{pp} for both perpendicular and parallel conditions for sample B is much broader than the standard P_b signal. The paramagnetic defect density more than doubles for sample B and decreases back to near the original level for the re-oxidized sample C. The g// value and the ΔB_{pp} for the re-oxidized sample C is between the value for the standard P_b center and the value post nitride deposition, indicating a gradual change back to the standard P_b character during re-oxidation.

The decrease in g// and increase of ΔB_{pp} is consistent with the introduction of N atoms into SiO_2, as a possible by-product result of the LPCVD nitride deposition. Jintsugawa et al.[120] have shown that ammonia dissociates at the surface of an oxide layer, leading to the diffusion of N atoms into the oxide. The formation of the oxynitride layer during APCVD silicon nitride deposition on a Si wafer with a native oxide was also observed by Hezel[121] using a combination of Auger electron loss spectroscopy and low energy electron loss spectroscopy. The g// value and the ΔB_{pp} for the re-oxidized sample C is between the value for the standard P_b center and the value post nitride deposition, indicating a gradual change from P_{bN} to P_b character during re-oxidation.

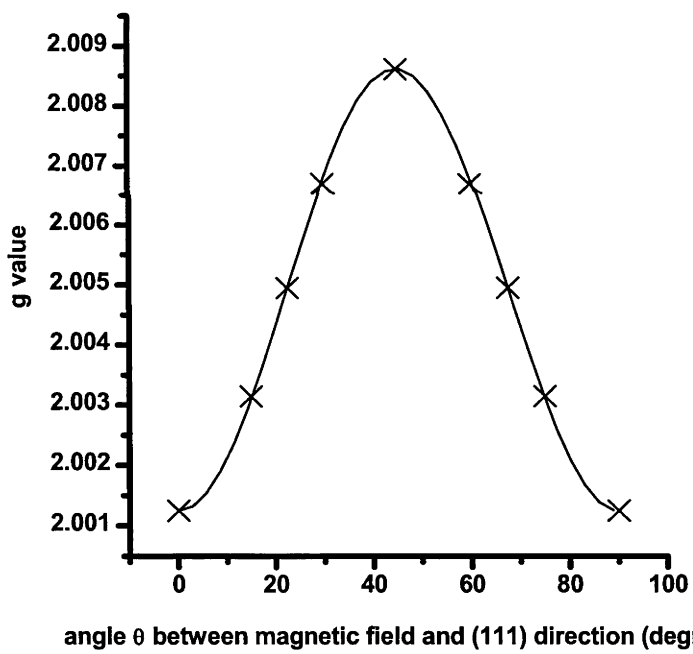

Figure 3.20. g values dependence on the angle θ between (111) direction and magnetic field direction

One possible explanation of the change of the defect properties is that the deposition of the nitride layer may lead to some nitridation of the $Si-SiO_2$ interface during the early stages of the deposition process. However, SIMS indicates nitridation of the top 10 nm of the oxide layer, but no significant nitridation at the $Si-SiO_2$ interface. Figure 3.21 shows the N depth profile in the

SiO_2 layer of a sample following nitride deposition. For this sample, 50 nm LPCVD Si_3N_4 had been deposited on a 50 nm thermally grown SiO_2 layer.

Therefore, it appears that the defect property change following nitride deposition is chiefly the result of increased interfacial stress, caused by the presence of a rigid nitride film with tensile stress on top of the oxide.

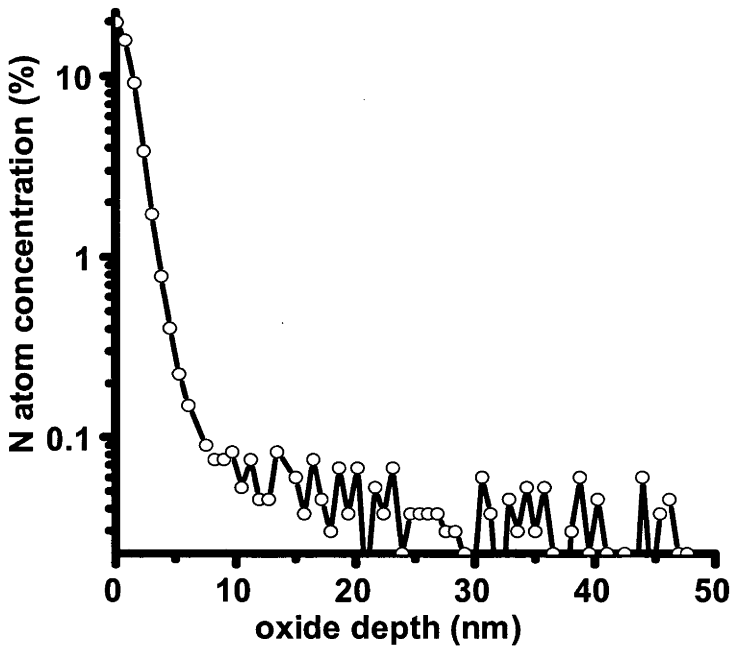

Figure 3.21. N atom distribution in SiO_2 layer at $Si_3N_4/SiO_2/Si$ stacks profiled by SIMS

3.3.2.3 Influence of LPCVD Si_3N_4 deposition on Si-SiO_2 interface defect distribution and Si surface recombination velocity

A comparison of the interface defect density within the Si forbidden bandgap between as oxidised samples, and samples that had a nitride layer deposited following oxidation and subsequently removed, is shown in figure 3.22 (C-V curves) and 3.23 (D_{it} distribution). Both samples had an FGA prior to metallisation and measurement. The oxide was 100 nm thick on and the nitride layer was about 50 nm thick. The nitride was deposited under standard conditions (775°C, 0.5 torr with an ammonia to DCS ratio of 4:1). Data from p type samples corresponds to the upper half of the band gap while data from n type samples corresponds to the lower half of the band gap. Mainly around the middle of the forbidden gap, the 'nitride removed' Si-SiO_2 interface shows a higher defect density than the as grown Si-SiO_2 interface.

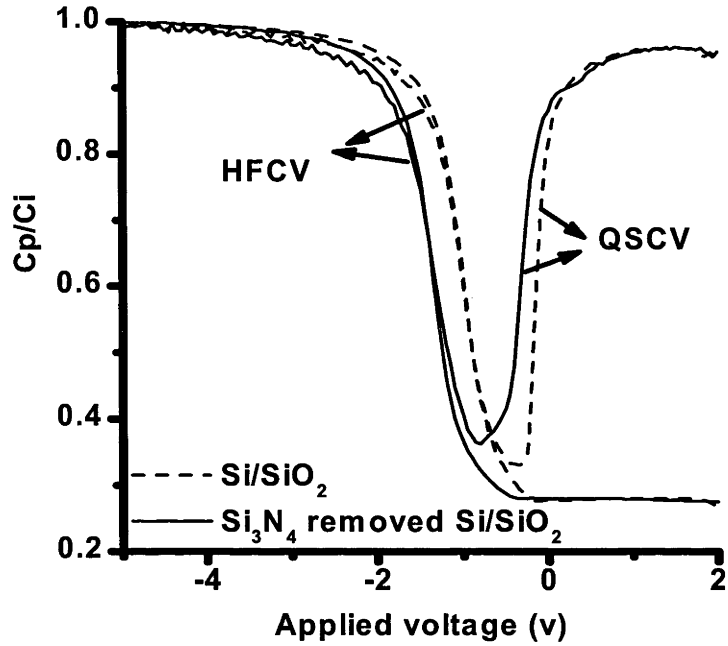

Figure 3.22. HFCV and QSCV curves of an as oxidised Si wafer (dashed line), and an oxidised wafer following nitride deposition and subsequent nitride removal (solid line). Both samples received an FGA prior to MOS structure formation.

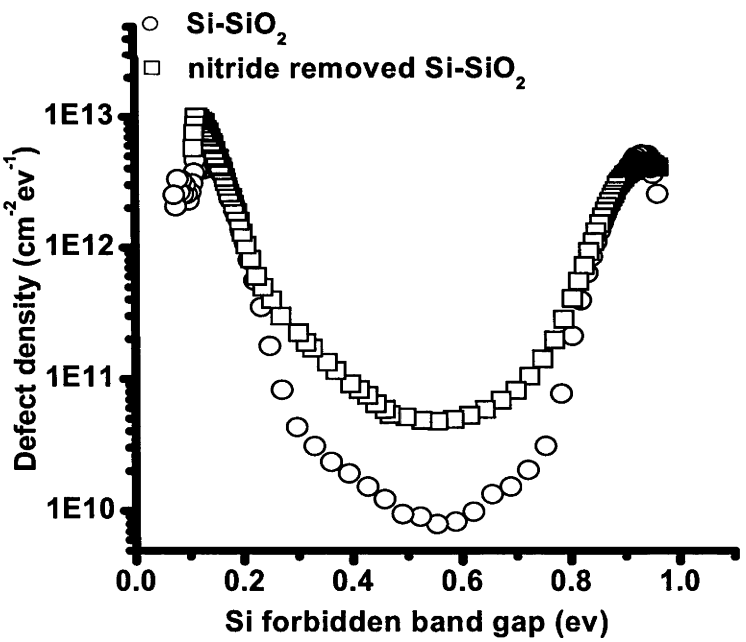

Figure 3.23. Comparison of defect density in the forbidden gap for the as grown Si-SiO_2 interface after FGA and the 'nitride removed Si-SiO_2' interface after FGA

LPCVD Si_3N_4 deposition on an oxidised Si sample also causes degradation of the Si surface properties with respect to minority carrier recombination. This is shown in Table 3.10 for both (100) and (111) wafers. The preparation of the samples was similar to that for the C-V

samples, with the difference that light phosphorus diffusion (with a sheet resistance of around 300 Ω/□ after thermal drive in) was done prior to oxidation, and that the oxide was only 50 nm thick.

	J_{oe} for (111) samples	J_{oe} (100) samples
$Si-SiO_2$	18	9
Si_3N_4 removed $Si-SiO_2$	30	19

Table 3.10. Emitter saturation current density (J_{oe} in fA/cm^2/side) on both (111) and (100) surfaces. The '$Si-SiO_2$' values were taken just after oxide growth and FGA. Si_3N_4 removed $Si-SiO_2$' values were measured on the same samples following subsequent nitride deposition, nitride removal and FGA.

All values in Table 3.10 come from well hydrogenated surfaces since, as before, all samples had an FGA prior to measurement. As can be seen from table 3.10, the trend for (111) and (100) surfaces is similar, although the (111) surfaces display consistently higher values of J_{oe}. The increase in J_{oe}, indicating an increase in surface recombination velocity, can be attributed to an increase in the interface defect concentration, as revealed by the C-V measurements. A change in the interface defect properties (in particular, their capture cross sections) could also have contributed to the increase in J_{oe}.

Figures 3.24 and 3.25 compare the effective lifetime of the as grown $Si-SiO_2$ interface and the 'nitride removed' interface for (100) and (111) Si substrates. The preparation of the samples was similar to that for the C-V samples, with the difference the oxide was only 50 nm thick. Note that the samples did not receive a phosphorus diffusion.

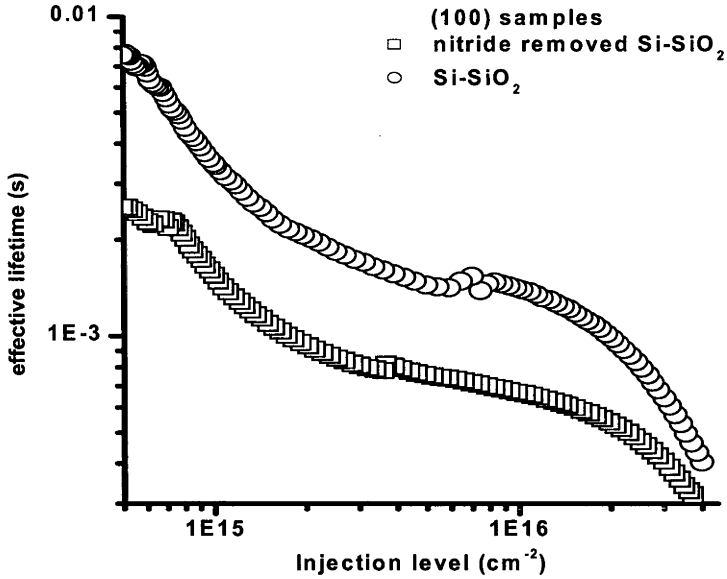

Figure 3.24. Comparison of effective lifetime for p type high resistivity (>100 Ω-cm), (100) Si/SiO_2 stacks. The rectangle symbols represent Si/SiO_2 stacks after nitride deposition and removal. The circle symbols represent as oxidized Si/SiO_2 stacks. All samples received an FGA before measurement.

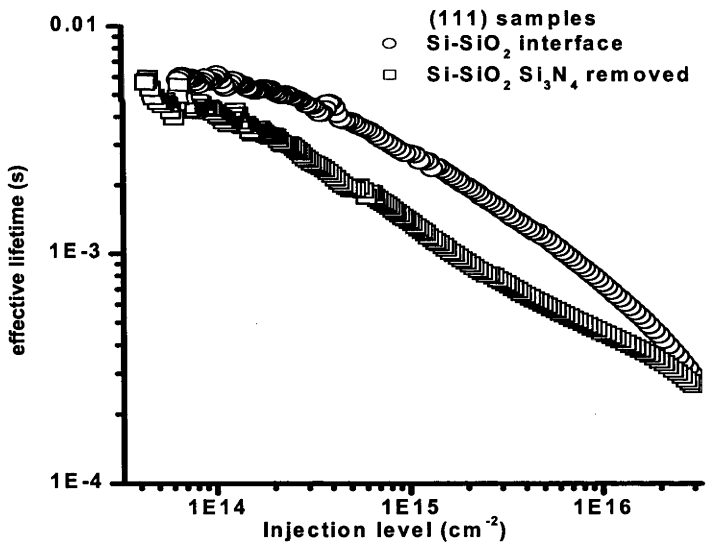

Figure 3.25. Comparison of effective lifetime for n type high resistivity (>100 Ω-cm), (111) Si/SiO_2 stacks. The rectangle symbols represent Si/SiO_2 stacks after nitride deposition and removed. The circle symbols as oxidized Si/SiO_2 stacks. All samples received a FGA before measurement.

For both p-type (100) and n-type (111) samples, the as-grown $Si-SiO_2$ interface displays higher lifetimes than the modified interface created by deposition and removal of a nitride layer.

The difference in lifetimes indicates changes in the electronic properties of the Si-SiO_2 interface as a result of nitride deposition.

Lifetime-voltage measurements were used to investigate the influence of LPCVD nitride deposition on the interface recombination properties in more detail. Figure 3.26 (a) shows the applied voltage dependent effective lifetime for SiO_2/Si, $Si_3N_4/SiO_2/Si$ and Si_3N_4/Si structures, while figure 3.26 (b) shows the corresponding J_{oe} curves. The nitride is 50 nm thick and oxide is about 50 nm thick. No phosphorus diffusion was performed on these samples. In accumulation and strong inversion, the effective lifetime is higher and the J_{oe} is lower for SiO_2/Si stacks than $Si_3N_4/SiO_2/Si$ stacks. When the Si surface is in accumulation or strong inversion, the charge in the insulator does not contribute to passivation since its effect is overwhelmed by the field effect generated from the applied bias.

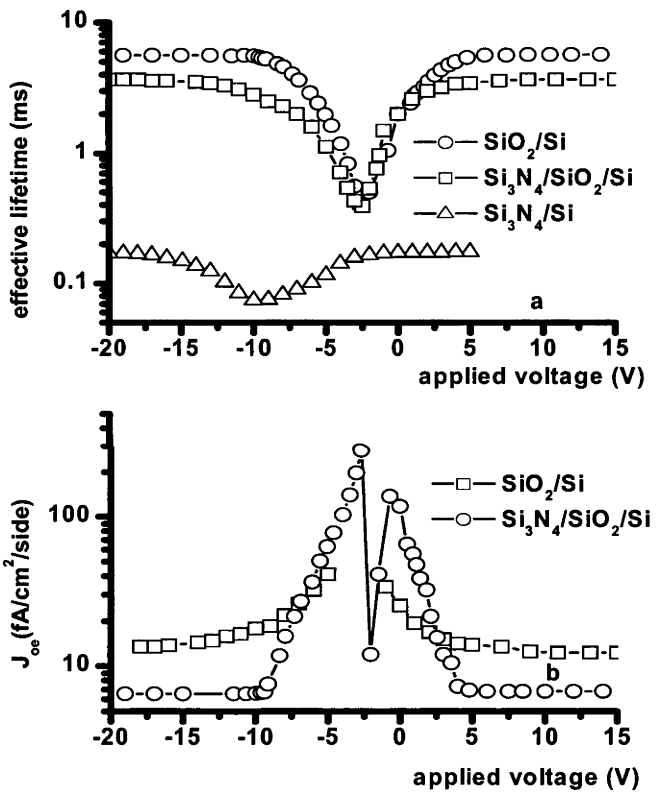

Figure 3.26. Effective lifetime (a) and J_{oe} (b) with applied voltage for SiO_2/Si, $Si_3N_4/SiO_2/Si$ and Si_3N_4/Si structures.

Table 3.11 shows S_{eff} values and Si bulk lifetimes for the SiO_2/Si and $Si_3N_4/SiO_2/Si$ structures. The calculation process was described in chapter 1. In accumulation and strong inversion, S_{eff} for the $Si_3N_4/SiO_2/Si$ structure is double the value for SiO2/Si stacks, while there is not a big difference in bulk lifetime for the two stacks. There may be two factors responsible for the higher S_{eff} for nitride stacks. One is due to the generation of new defects during LPCVD nitride deposition. The other one could be the loss of hydrogen during LPCVD nitride

deposition. The loss of hydrogen may electronically activate some originally bonded defects. This is discussed in more detail in later sections.

	S_{eff} at accumulation (cm/s)	S_{eff} at strong inversion (cm/s)	Bulk lifetime (ms)
SiO_2/Si	1.8	1.7	9.6
$Si_3N_4/SiO_2/Si$	3.6	3.3	9.2

Table 3.11. Effective surface recombination velocity (S_{eff}) in accumulation and strong inversion and the Si bulk lifetime for SiO_2/Si, $Si_3N_4/SiO_2/Si$ stacks at the injection level of 4×10^{15} /cm^3.

The effective lifetime for Si_3N_4/Si stacks shown in figure 3.26 (a) is much lower than for nitride stacks with oxide, which again indicates that direct deposition of LPCVD nitride on Si will damage the Si bulk and surface. When no bias is applied to the Si_3N_4/Si stacks, the lifetime is already saturated, which indicates that the surface is already in strong inversion. This effect is due to the positive charge in the nitride layer. Without an oxide, the lifetime-voltage curve reaches its lowest point at about –10 V, while with oxide the lowest lifetime occurs at about –2.5 V.

3.3.2.4 Thermal stability of nitride removed Si-SiO_2 interface

In this section, the thermal stability of the modified Si-SiO_2 interface (obtained after nitride deposition and removed) is studied and compared with the as grown Si-SiO_2 interface by lifetime and C-V measurements. The sample preparation was mentioned in section 3.3.2.1. After oxide growth and LPCVD nitride deposition, the nitride layer was removed from selected samples in order to allow a direct comparison with the as oxidized samples. Figures 3.27 and 3.28 show effective lifetimes for (100) and (111) as grown and modified ('nitride removed') Si-SiO_2 interfaces, after an RTA at 550°C for 3 min in dry nitrogen gas. Samples received the same treatments as samples used in figure 3.24 and 3.25.

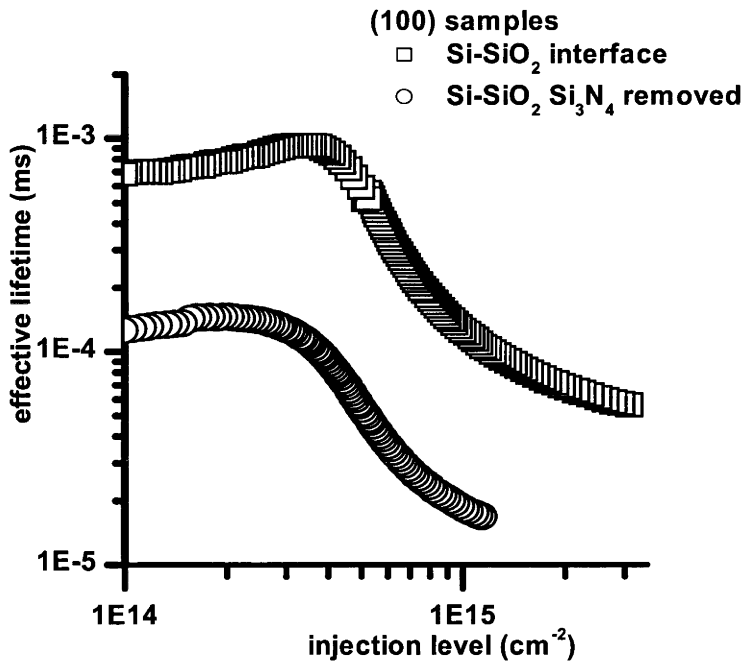

Figure 3.27. Effective lifetime for p type high resistivity (>100 Ω-cm), (100) Si/SiO_2 stacks and nitride removed Si/SiO_2 stacks after 550°C RTA for 3 min

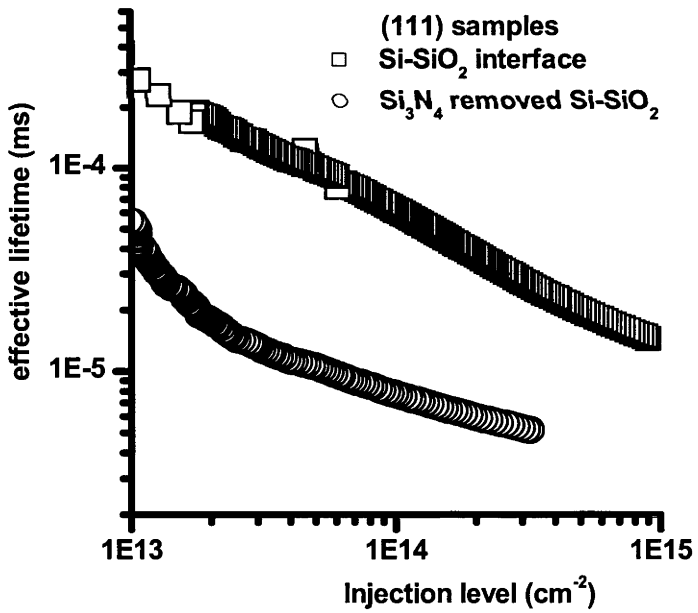

Figure 3.28. Effective lifetime for n type high resistivity (>100 Ω-cm), (111) Si/SiO_2 stacks and nitride removed Si/SiO_2 stacks after 550°C RTA for 3 min

Compared with the as oxidised results in figures 3.24 and 3.25, the effective lifetime for both the (100) and (111) samples has decreased dramatically. The changes to the $Si-SiO_2$

interface, effected by the deposition of the nitride layer, result in a more rapid de-passivation rate of the interface compared to the as-grown interface. The interface on (111) samples shows a faster de-passivation rate than the (100) interface. The rapid degradation in response to thermal annealing of the (111) $Si-SiO_2$ interface is probably the result of the higher defect density of this interface. C-V results show that at mid gap, the defect density post FGA for (111) Si/SiO_2 interfaces is about $4.2\times10^{10}/cm^2$, in contrast to the mid gap defect density of around 7.9×10^9 $/cm^2$ for (100) interfaces, as shown in chapter 2.

Figures 3.29 and 3.30 show the changes in J_{oe} following isothermal and isochronal RTAs. All values at the no annealing stages (0 minutes on the graph) come from well hydrogenated surfaces (ie. just after an FGA). These results are consistent with those of table 3.10. The trend for (111) and (100) surfaces is similar, although the (111) surfaces display consistently higher values of J_{oe}. These results are consistent with the increase in interface defects detected by EPR and C-V.

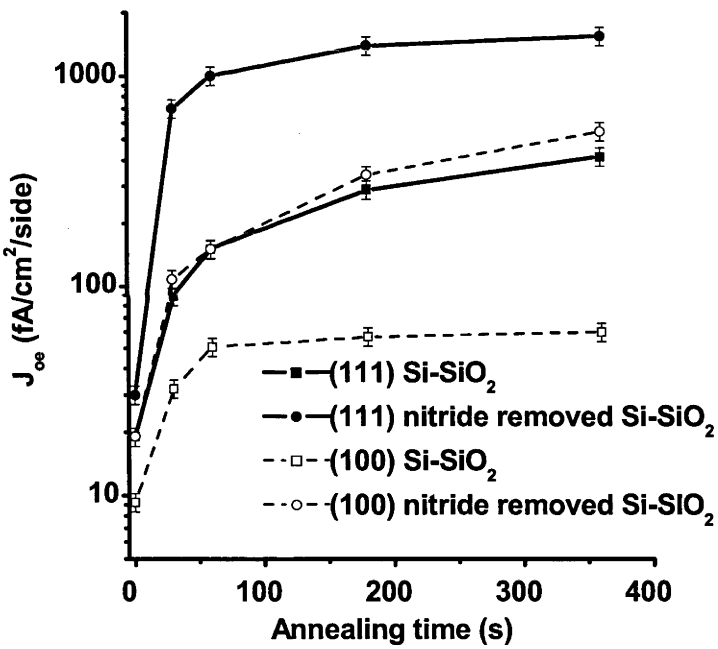

Figure. 3.29. J_{oe} values after isothermal RTAs at 550°C. Curves for 'Si-SiO_2' are for oxidized samples without nitridation. Curves labeled 'nitride removed Si-SiO_2' are for oxidised samples with subsequent nitride deposition, nitride strip and FGA.

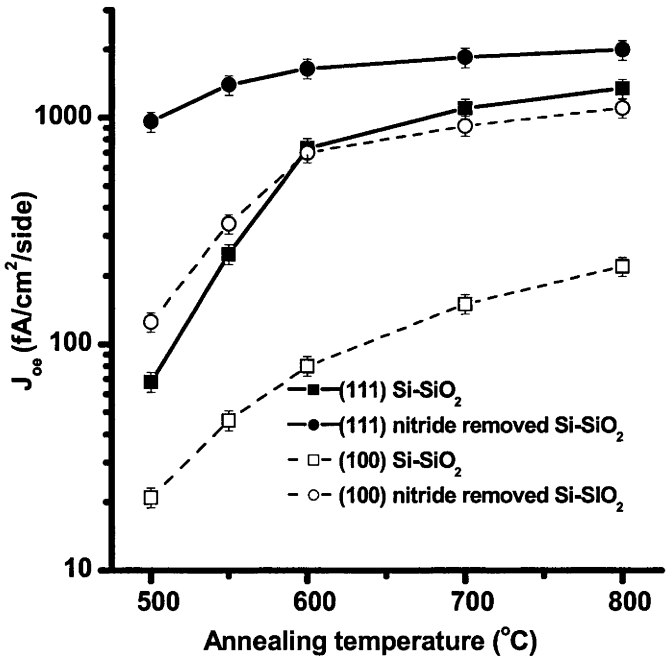

Figure. 3.30. J_{oe} values after isochronal RTAs for 3 minutes. Curves for 'Si-SiO_2' are for oxidized samples without nitridation. Curves labeled 'nitride removed Si-SiO_2' are for oxidised samples with subsequent nitride deposition, nitride strip and FGA.

Figures 3.31 and 3.32 show the quasi-static C-V (QSCV) curves for as oxidised samples after isothermal RTAs at 550°C for 90-360 seconds and isochronal RTAs at 550°C to 800°C for 3 minutes.

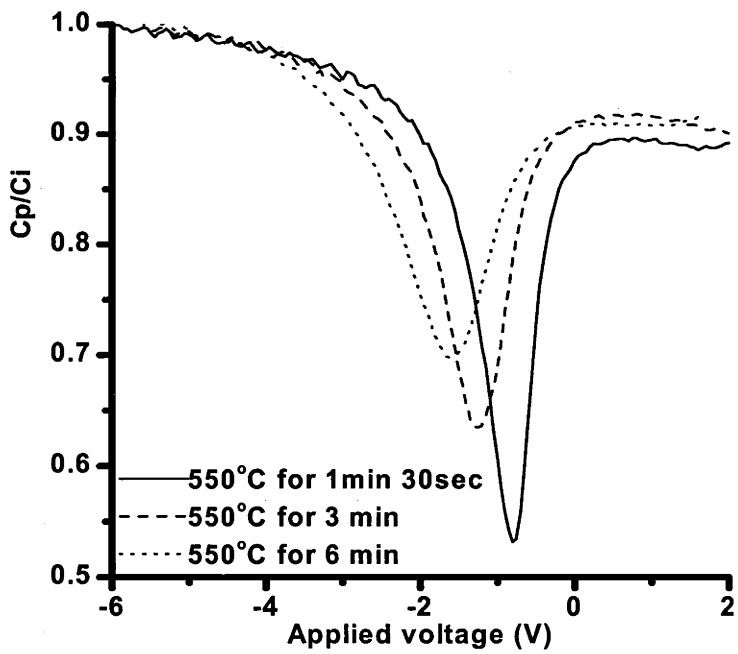

Figure 3.31 QSCV curves for p type MOS stacks after RTA at 550°C from 1.5 min to 6 min

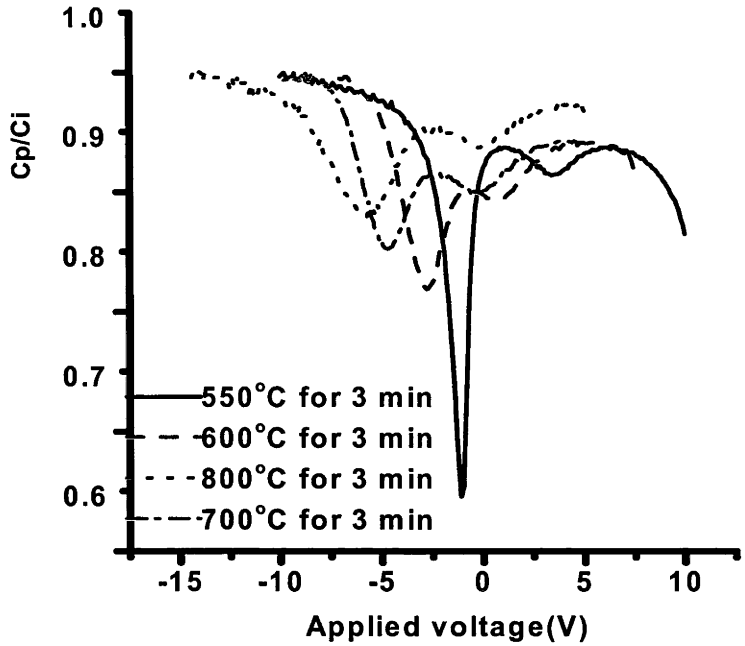

Figure 3.32 QSCV curves for p type MOS Stacks after RTA at 550°C to 800°C for 3 min

As either the annealing time or the annealing temperature increases, the QSCV curves shift to a more negative voltage, indicating an increase in the density of positive interface charges. The ratio of measured capacitance to insulator capacitance (Cp/Ci) gives an indication of the interface defect density. As annealing time or temperature increase, the lowest value of Cp/Ci increases, indicating that more interface defects are generated due to a loss of hydrogen at the interface. Figure 3.32 shows that RTA treatments distort the QSCV curve and introduce another dip at accumulation. This dip may be related to stress at the interface[122].

Figures 3.33 and 3.34 show a comparison of charge density and figures 3.35 and 3.36 show a comparison of mid gap defect density between as oxidised and nitride removed samples, after isothermal and isochronal anneals.

The positive charges are believed to be fixed in the oxide layer within 2-3 nm of the Si surface; this layer has been shown to be non-stoichiometric and to contain the interface defects[123]. Some of the interface defects may be positively charged and may be responsible for the flat band voltage shift in the negative direction.

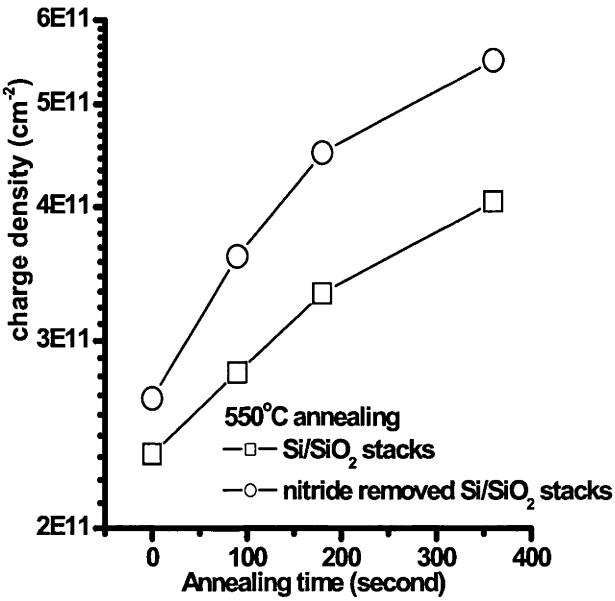

Figure 3.33 charge density of as oxidized and nitride removed samples after RTAs at 550°C from 1.5 min to 6 min.

With an increase in annealing time and temperature, the mid gap interface defect density and interface charge density increase. Nitride removed samples display a higher defect density, in good agreement with the lifetime results. The mid gap defect density curves appear to saturate after 3 minutes (figure 3.31) and at 800°C (figure 3.36), however, the charge density does not show a similar saturation trend in figures 3.33 and 3.34.

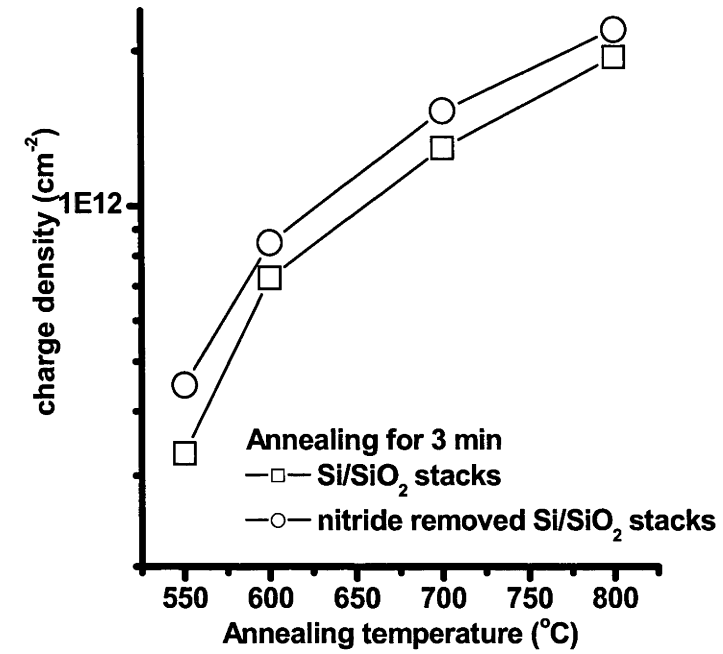

Figure 3.34 charge density of as oxidized and nitride removed samples after RTAs at 550°C to 800°C for 3 minutes.

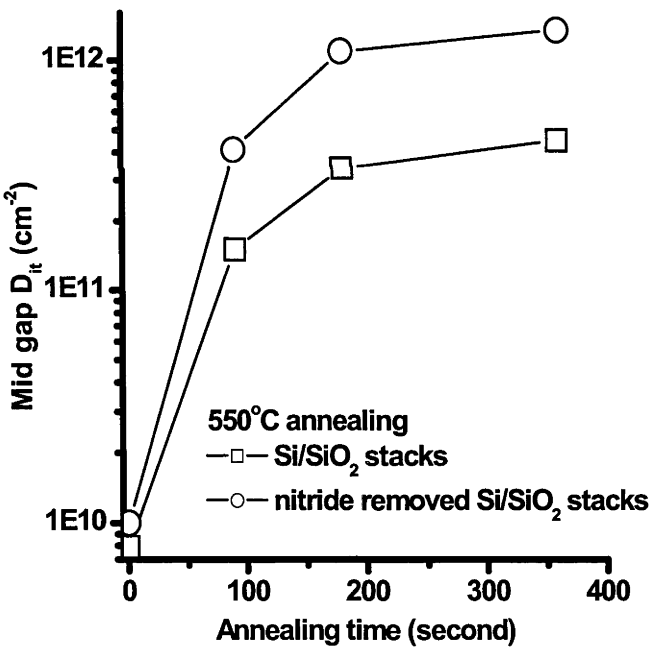

Figure 3.35. Mid gap defect density for Si/SiO_2 Stacks and nitride removed Si/SiO_2 stacks after RTA 550°C from 1.5 min to 6 min

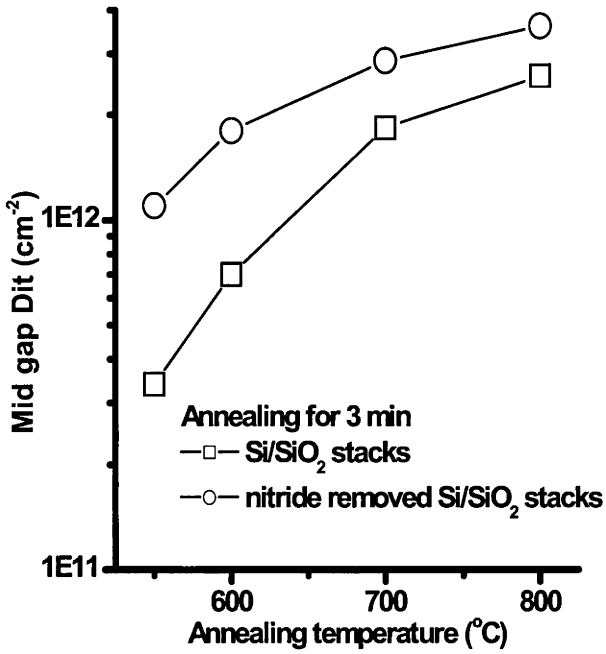

Figure 3.36 Mid gap defect density for Si/SiO_2 Stacks and nitride removed Si/SiO_2 stacks after RTA 550°C to 800°C for 3 min

3.3.3 LPCVD Si_3N_4 deposition influence on passivation of Si-SiO_2 interface

In this section, the effect of LPCVD Si_3N_4 deposition on the interface properties of oxidised silicon wafers is studied in more detail. The effect of varying the ammonia to DCS ratio during nitride deposition is discussed. The influence of oxide and nitride thickness on the Si-SiO_2 interface recombination velocity is studied. The thermal stability of LPCVD $Si_3N_4/SiO_2/Si$ stacks is studied and compared with that of oxidised silicon wafers.

3.3.3.1 Experimental details

Lifetime and C-V measurements were used for checking the influence of LPCVD Si_3N_4 deposition on Si-SiO_2 interface defect density and recombination velocity. Float-zoned, p-type, ~100 Ω-cm, (100) Si wafers were used for carrier lifetime measurements. Cz, p-type, 10-23 Ω-cm, (100) Si samples and Cz, n-type, 3-10 Ω-cm, (100) samples were used for CV measurements.

After Si etching and standard RCA cleaning, the wafers for lifetime measurements were given a light phosphorus diffusion (R~ 300-400 Ω/□ after thermal drive in). All samples were passivated with a thermally grown oxide, followed by a N_2 in-situ anneal at 1000°C for 30 minutes. Hydrogenation of the $Si-SiO_2$ interfaces was achieved using a FGA at 400°C for 30 minutes. De-hydrogenation was achieved using Rapid Thermal Anneals at 800°C for 3 minutes in dry nitrogen.

LPCVD Si_3N_4 depositions were carried out at 775°C and 0.5 torr with various ammonia and DCS flow rate. Nitride layers were removed from selected samples, followed by a FGA at 400°C for 30 minutes.

For samples used for C-V measurements, all samples received a Si etch and RCA cleaning. All samples were passivated with a thermally grown oxide, subsequently followed by a N_2 in-situ anneal at 1000°C for 30 minutes. Hydrogenation of the $Si-SiO_2$ interfaces was achieved using a FGA at 400°C for 30 minutes. LPCVD Si_3N_4 depositions were carried out at 775°C and 0.5 torr. Nitride layers were removed from selected samples, followed by a FGA at 400°C for 30 minutes. One side of the insulator was carefully removed by HF fume and ~80 nm Al was deposited through a shadow mask with an area of 4.7×10^{-3} cm^{-2}. Ohmic contact by Ga-In was pasted to the Si bulk.

3.3.3.2 Effect of nitride thickness on Si surface recombination

Figure 3.37 shows the J_{oe} values for two oxidised Si samples, A (in figure 3.37(a)) and B (in figure 3.37(b)), after different processes. Sample A had initially been hydrogenated with an FGA, while sample B had been de-hydrogenated with an 800°C RTA (step 1). Subsequently, silicon nitride was deposited on both samples in three separate steps, resulting in a nitride layers of increasing thickness. The total nitride thickness at steps '2', '3', '4' is around 3, 31 and 53 nm respectively. The nitride layers were not removed between the three depositions. In step 5, the nitride layers were removed in hot phosphoric acid at 170°C. Finally, both samples received an FGA to re-hydrogenate the interface at step 6.

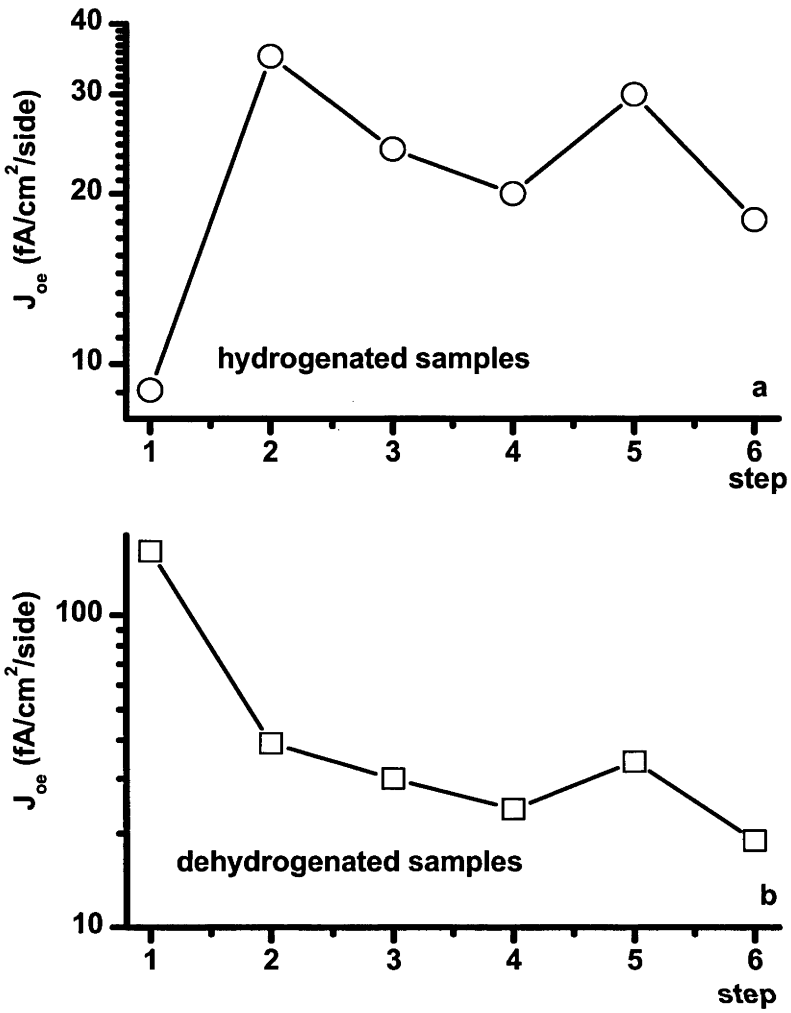

Figure 3.37. J_{oe} values for samples A and B after different thermal steps. Step 1: Oxidization and FGA at 400°C for 30 min on sample A, RTA at 800°C for 3 min on sample B. Steps 2 to 4: Nitride deposition for 1, 6 and 5 minutes, respectively. Step 5: Nitride removal using phosphoric acid. Step 6: FGA.

As shown in figure 3.37(a), a 1 min deposition of about 3 nm Si_3N_4 increases J_{oe} from 9 to 35 fA/cm^2 per side for sample A. For comparison, a simulated deposition was carried out in the LPCVD nitride deposition reactor for 1 min on another sample (sample C). The simulated deposition involved admitting pure N_2 instead of ammonia and DCS, so that no deposition took place. For this sample, J_{oe} increased from 9 to 20 fA/cm^2 per side. The increase of J_{oe} for sample C is due to a loss of hydrogen from the Si-SiO_2 interface, as a fraction of the interface defects which are initially terminated with hydrogen lose their hydrogen atoms, changing the defects from electrically inactive to electrically active. However, this type of treatment does not significantly affect the density or the fundamental properties of interface defects, except for their bonding state[71]. The larger increase in J_{oe} of sample A compared to sample C again indicates that the nitride deposition has additionally resulted in a change in the density and the

physical or electronic properties of the defects at the Si-SiO_2 interface, which has been explained in previous sections.

A comparison of the J_{oe} values of samples A and B following a 1 minute nitride deposition indicates that hydrogen also plays an important role during this initial stage of the deposition.

Sample B had nearly the same as-oxidized J_{oe} value and sheet resistance as samples A and C. After an RTA at 800°C for 3 min in N_2, its J_{oe} increased to 160 fA/cm^2 per side, which represents a nearly completely de-hydrogenated Si-SiO_2 interface for this sample. After a 1 min LPCVD nitride deposition, J_{oe} decreased to 39 fA/cm^2 per side, similar to sample A. The passivation of this initially de-passivated sample is due to hydrogen made available by the nitride deposition process. The change in the fundamental properties of the Si-SiO_2 interface as a result of nitridation of both samples A and B is also evidenced by the higher J_{oe} values at step 6 compared to step 1.

Figure 3.38 shows the dependence of the mid gap D_{it} and J_{oe} on the nitride thickness for $Si_3N_4/SiO_2/Si$ stacks. The oxide thickness was 50 nm. The nitride layer was removed and the samples were given a FGA just before the C-V measurements. It can be seen that the increase in mid gap D_{it} and J_{oe} occurs in the initial stages of nitride film deposition (during the first 5-10 nm).

As mentioned previously, it appears that the increase in D_{it} and J_{oe} following nitride deposition is chiefly the result of increased interfacial stress, caused by the presence of a rigid nitride film with tensile stress on top of the oxide. The magnitude of the interfacial stress is not significantly affected by the thickness of the nitride film above a certain critical thickness. In addition, nitridation of the surface region of the SiO_2 layer, which causes an increase in rigidity of the SiO_2 film may play a role while for very thin oxides (~20 nm or less), interface nitridation could have a significant impact on defect generation as well.

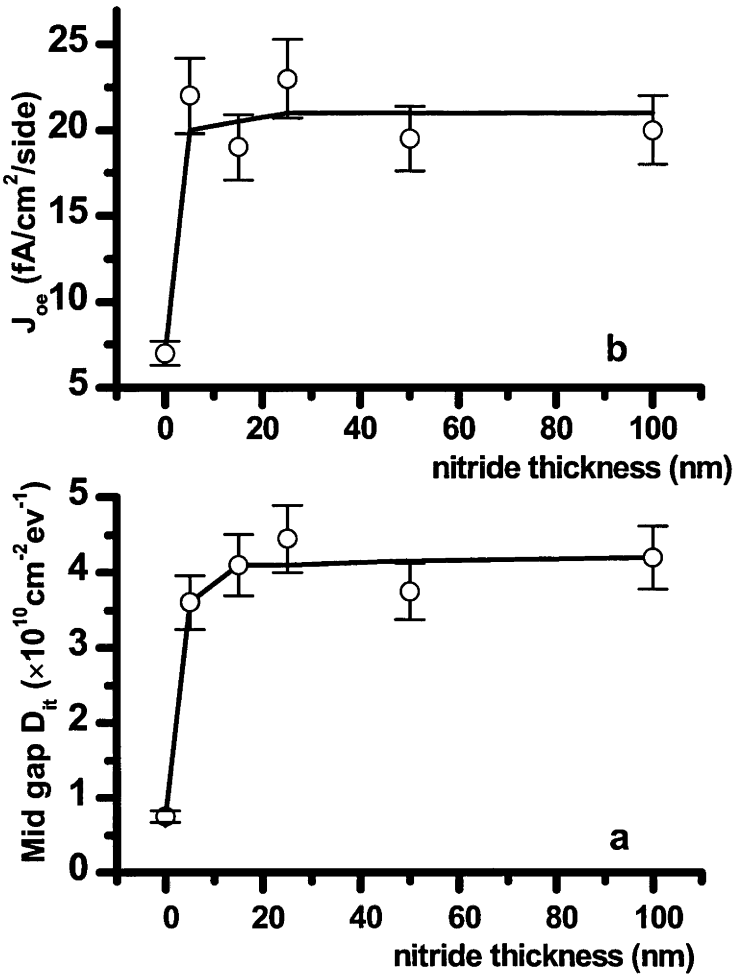

Figure 3.38. Mid gap Dit (a) and J_{oe} values (b) for SiO_2/Si sample after nitride deposition, nitride removal and FGA. The oxide is 50 nm thick. The lines are guides to the eye.

3.3.3.3 Effect of ammonia to DCS flow ratio during deposition on Si surface recombination

The degree of change in the properties of the Si-SiO_2 interface as a result of nitride deposition may be influenced by the choice of LPCVD Si_3N_4 deposition parameters. The effect of deposition temperature and ammonia to DCS flow ratio were investigated. Because of limitations on the LPCVD system used for the experiments, the deposition temperature could only be varied between 750°C to 800°C. Little influence of surface recombination was observed within this temperature change. However, the ammonia to DCS flow ratio was found to have a significant effect.

Sample preparation was similar to the previous section except that for some samples, the ammonia flow rate was varied between 120 and 210 scc/m while the DCS flow rate was kept constant at 30 scc/min to investigate the effect of the gas flow ratio on the interface properties.

Figure 3.39 shows the influence of ammonia to DCS ratio on the J_{oe} values of samples immediately after nitride deposition, and following a subsequent removal of the nitride in phosphoric acid.

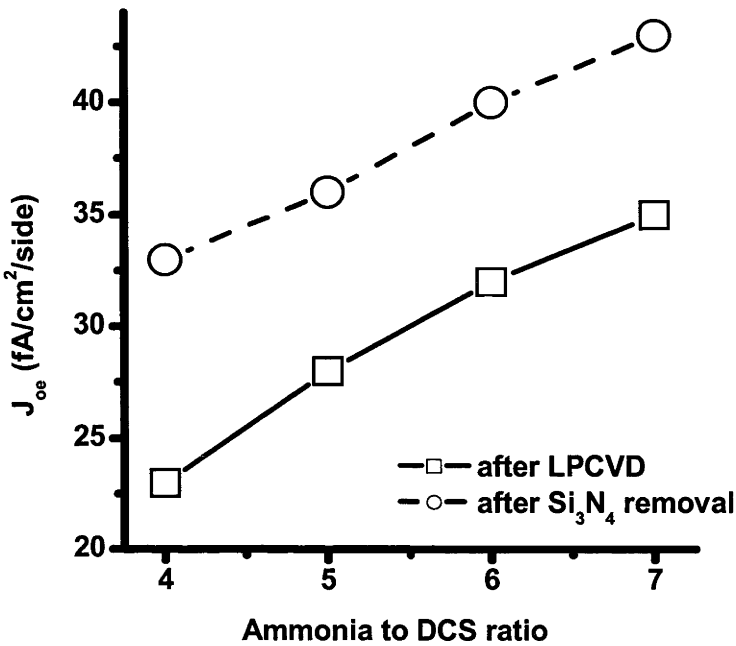

Figure 3.39. Dependence of emitter saturation current density J_{oe} on the ammonia to DCS flow ratio (a) immediately after LPCVD deposition of ~50 nm of Si_3N_4 on oxidised Si (solid line); (b) following subsequent removal of the nitride layer (dashed line)

It can be seen that an increase in the ammonia to DCS ratio leads to a monotonic increase in J_{oe} values. A possible explanation of this result is that the change of flow ratio could influence the magnitude of the stress in the nitride layer and hence affect the Si surface recombination velocity[124]. Following removal of the nitride film, the trend in the J_{oe} values remains unchanged, although all J_{oe} values have increased.

To further investigate the influence of LPCVD gas flow ratio on the interface properties, two extreme surface conditions were investigated. The first is the hydrogenated interface, which is realized by an FGA at 400°C for 30 min. The second is the completely or nearly completely dehydrogenated interface, which is realized by an RTA in N_2 flow at 800°C for 3 min. The ammonia to DCS flow ratio dependence of J_{oe} under hydrogenated and dehydrogenated conditions is shown in figures 3.40 and 3.41, respectively. Under both conditions, a high ammonia to DCS ratio results in greater degradation of the electronic properties of the Si surface.

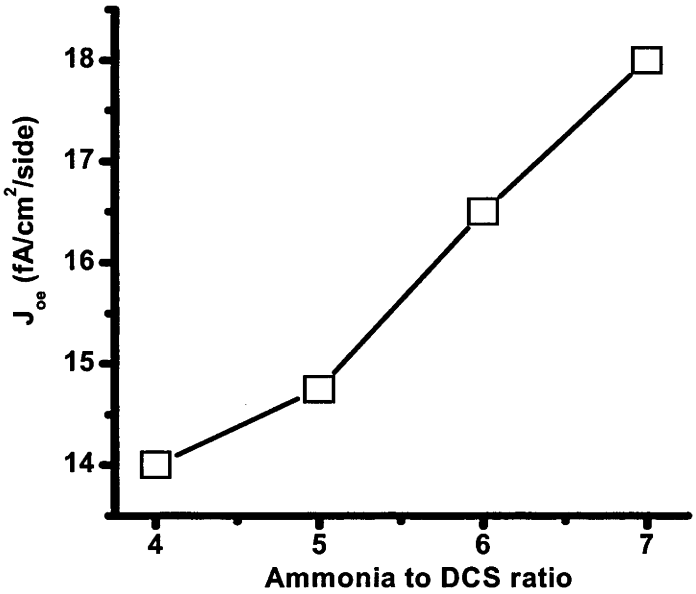

Figure 3.40. Dependence of emitter saturation current density J_{oe} on the ammonia to DCS flow ratio for the hydrogenated oxynitride interface

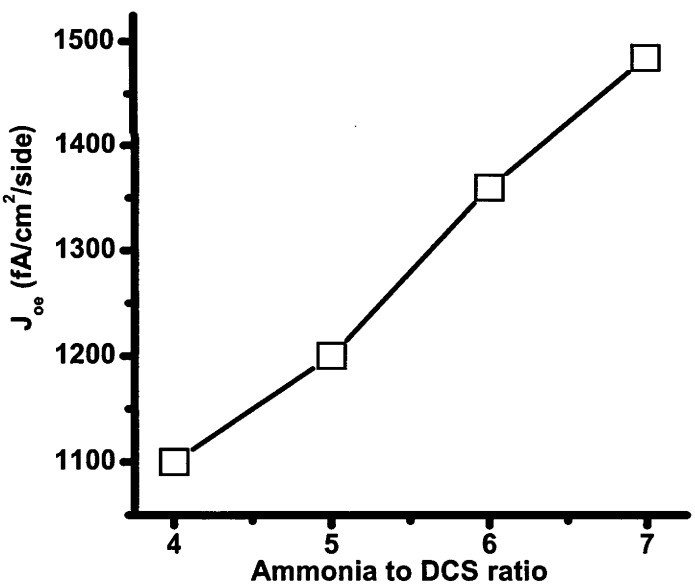

Figure 3.41. Dependence of emitter saturation current density J_{oe} on the ammonia to DCS flow ratio for the dehydrogenated oxynitride interface

3.3.3.4 Effect of charge on Si surface recombination

As shown in figure 3.37, deposition of a thicker Si_3N_4 layer (steps 3 and 4) results in a further improvement of the passivation of the Si-SiO_2 interface. These improvements may be due both to the passivation of the interface by hydrogen from the LPCVD nitride film, and the effect of positive charges in the nitride film[116]. Both figure 3.37 and 3.39 also show that removal of the nitride layer degrades interface passivation. This degradation is due to the removal of the positive charges in the nitride film and the oxide/nitride interface, which helped to provide interface passivation. Figure 3.10 demonstrates the high frequency capacitance-voltage curves for metal-LPCVD Si_3N_4-Si and metal-SiO_2-Si structures, more negative flat band voltage was observed from the nitride stacks due to the charge in nitride film.

3.3.3.5 Effect of oxide thickness on Si surface recombination

To check the influence of oxide layer thickness on the degradation of Si surface after nitride deposition, oxide thicknesses in the range of 30-110 nm were prepared on separate samples. All other sample preparation details are similar to those in the previous section.

Figure 3.42 clearly shows that the presence of an intermediate oxide is effective at reducing mid gap D_{it} and J_{oe}, and also shows that there is a good correlation between the two parameters. Direct deposition of the nitride film with tensile stress on Si will result in a strained interface with high recombination velocity. The introduction of a compressively stressed oxide layer between Si and Si_3N_4 can reduce the interface stress and results in an interface with a lower defect density.

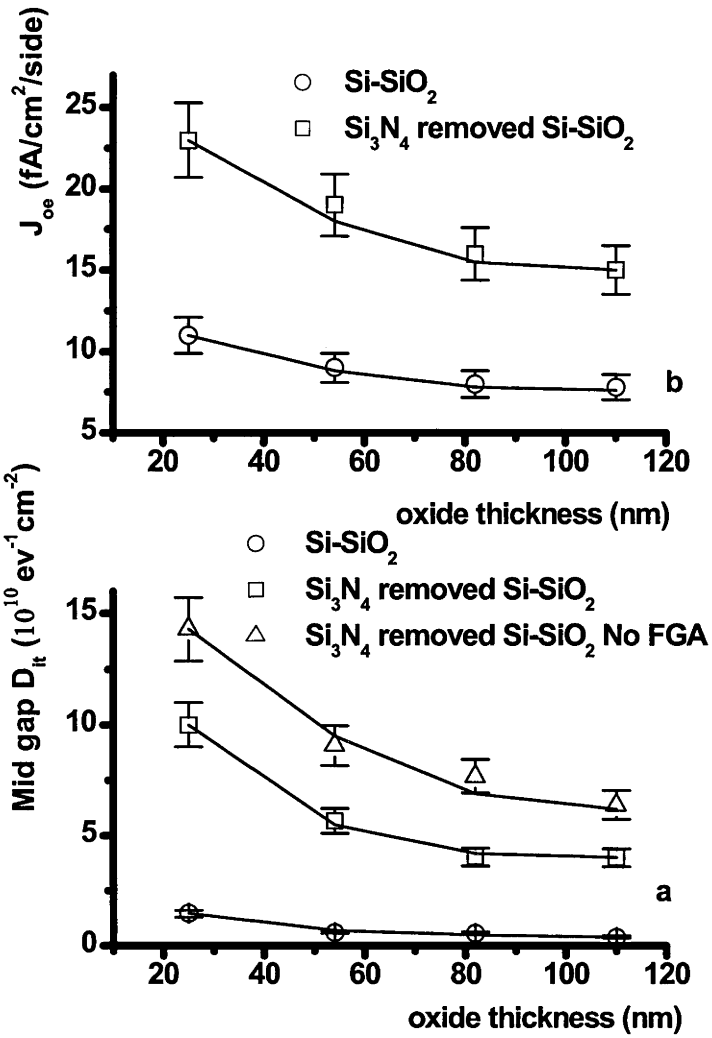

Figure 3.42 Oxide thickness dependence of (a) mid gap D_{it} and (b) J_{oe} for the as-grown Si-SiO_2 interface (circles) and the Si-SiO_2 interface following nitride deposition and subsequent removal (squares and triangles). All samples received an FGA prior to MOS structure formation (for C-V measurements) and measurement except for the samples represented by the triangles. The lines are guides to the eye.

With a ~110 nm oxide, the mid gap interface defect density after nitride deposition and removal is about 6.4×10^{10} $cm^{-2}eV^{-1}$, around 3 times lower than that of the sample with a very thin oxide. A subsequent FGA after nitride removal further reduces the interface defect density, because hydrogen bonds with many of the remaining interface defects. However, figure 3.42 shows that the mid gap D_{it} and J_{oe} values for all samples following nitride removal and FGA are still much higher than the corresponding values of the as oxidized and FGAed Si-SiO_2 interface. A similar trend of D_{it} as a function of oxide thickness was observed by Xu and Kapoor[125].

3.4 Thermal Stability of $Si_3N_4/SiO_2/Si$ stacks

3.4.1 Experimental details

Lifetime measurements were carried out to investigate the thermal stability of $Si_3N_4/SiO_2/Si$ stacks. Float-zoned, p-type, ~100 Ω-cm, (100) Si wafers were used for carrier lifetime measurements. To check the influence of an in-situ anneal in N_2 on the interface properties, n type, FZ, (111), ~100 Ωcm Si samples were used. After Si etching and a standard RCA cleaning, the wafers were given a light phosphorus diffusion (R~ 300-400 Ω/□ after thermal drive in). All samples were passivated with a thermally grown 50 nm oxide, followed by a N_2 in-situ anneal at 1000°C for 30 minutes selected samples. Hydrogenation of the $Si-SiO_2$ interfaces was achieved using a FGA at 400°C for 30 minutes. De-hydrogenation was achieved using Rapid Thermal Anneals at 800°C for 3 minutes in dry nitrogen. 50 nm LPCVD Si_3N_4 depositions were carried out on selected samples at 775°C and 0.5 torr with an ammonia flow rate of 120 scc/min and a DCS flow rate of 30 scc/min.

To compare the thermal stability of LPCVD $Si_3N_4/SiO_2/Si$ stacks and oxidised silicon wafers, isothermal (550°C up to 360 seconds) and isochronal (500°C to 800°C for 180 seconds) RTAs were carried out on samples.

3.4.2 Comparison of thermal stability between $Si_3N_4/SiO_2/Si$ stacks and SiO_2/Si stacks

Figures 3.43 and 3.44 compare the thermal stability of $Si_3N_4/SiO_2/Si$ stacks and oxidised, initially hydrogenated Si samples. The nitride/oxide stacks display better thermal stability during both isothermal annealing and isochronal annealing than samples with an oxide only. The improved thermal stability of the nitride/oxide stack is likely to be due to hydrogen in the nitride layer, in the form of N-H and Si-H bonds. During thermal annealing, some of these hydrogen bonds (particularly the less stable Si-H bonds) in the nitride layer dissociate and the liberated hydrogen diffuses towards the $Si-SiO_2$ interface, where it passivates interface defects. The amount of hydrogen released in this way is small compared with the total bonded hydrogen concentration, since little change in hydrogen content is observed by MIR-FTIR at annealing temperatures below the deposition temperature and annealing times up to several hours. The gradual release of hydrogen from the nitride film means that it is possible to carry out some

thermal processing steps following nitride layer deposition with only a small degradation of surface passivation.

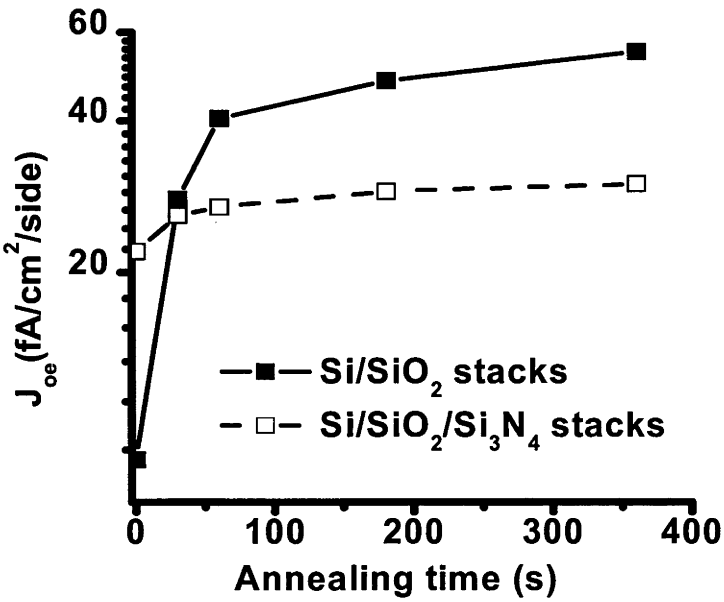

Figure 3.43. Emitter saturation current density (J_{oe}) isothermal (at 550°C) RTA curves for (a) hydrogenated (100) Si / SiO_2 stacks (solid line); (b) (100) Si / SiO_2 / Si_3N_4 stacks (dashed line)

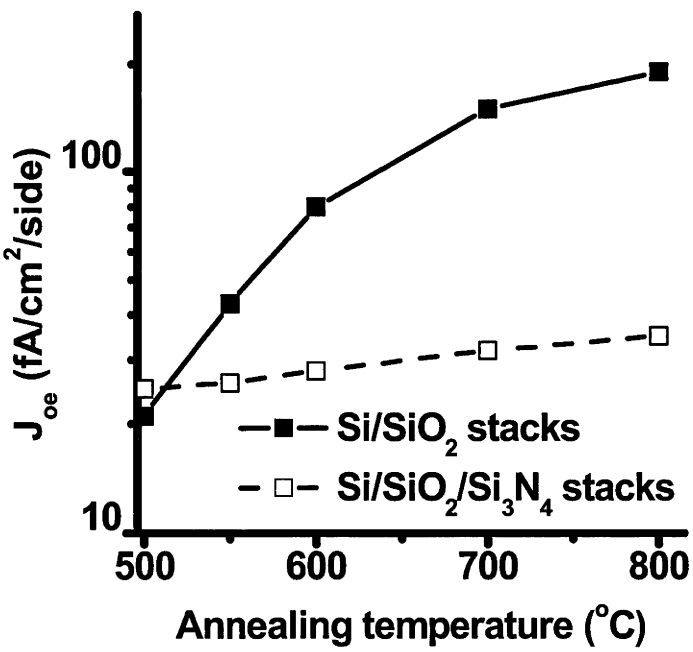

Figure 3.44. Emitter saturation current density (J_{oe}) isochronal (3 minutes) RTA curves for (a) hydrogenated (100) S /SiO_2 stacks (solid line); (b) (100) Si/SiO_2/Si_3N_4 stacks (dashed line)

3.4.3 Comparison of thermal stability of $Si_3N_4/SiO_2/Si$ stacks with and without insitu anneal in N_2

In chapter 2, the effect of post oxidation in-situ annealing in N_2 was investigated and found to effectively reduce the Si surface recombination velocity and increase the thermal stability. The effect of post oxidation in-situ annealing in N_2 was studied for $Si_3N_4/SiO_2/Si$ stacks as well. N type, FZ, (111), ~100 Ωcm Si samples were used. Experimental details are given in section 3.4.1. Figures 3.45 and 3.46 show the effect of an in-situ N_2 anneal on nitride stacks after 3 minutes isochronal and 550°C isothermal RTAs. The effective surface recombination velocity was calculated from equation 1.8 assuming an infinite bulk lifetime.

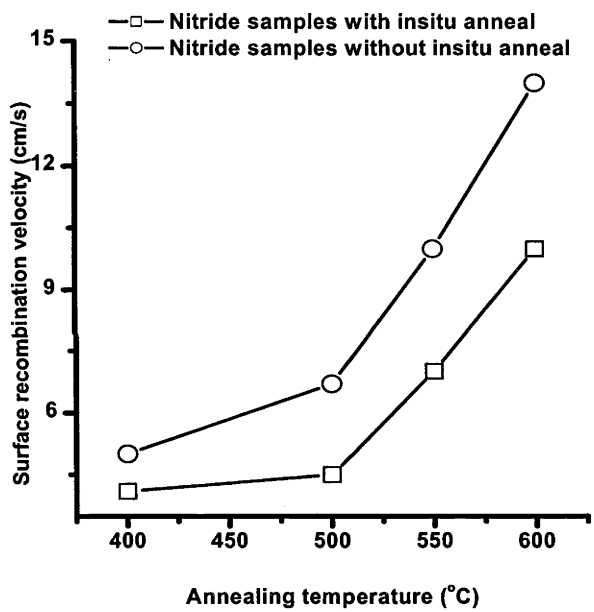

Figure 3.45. isochronal anneal on $Si_3N_4/SiO_2/Si$ stacks for 3 minutes in N_2. All samples are undiffused.

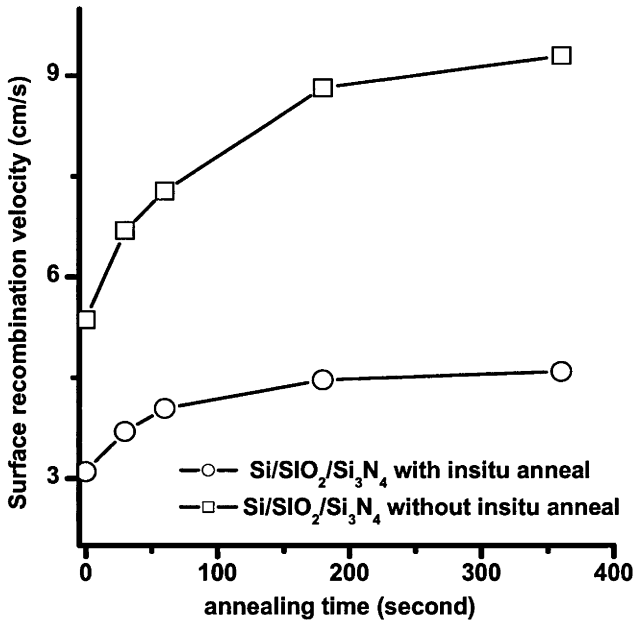

Figure 3.46. isothermal anneal on $Si_3N_4/SiO_2/Si$ stacks at 550°C in N_2

3.5 $Si_3N_4/SiO_2/Si$ stacks Implications for solar cell design

Figure 3.47 shows the effect of oxide thickness on the solar weighted (AM1.5G spectrum) reflectance of planar $Si_3N_4/SiO_2/Si$ stacks with optimised nitride layer thickness, encapsulated behind glass with a pottant such as EVA. The refractive index of the pottant, glass and oxide layer was set to 1.46 (independent of wavelength) while n=2.0 was used for the nitride. The reflectance changes relatively slowly at first, but then increases more rapidly as the oxide thickness is increased beyond 20 nm. It is therefore clear that the determination of optimal oxide thickness involves a compromise between optical and electronic properties. An oxide thickness of ~20 nm is likely to be optimal in most situations as it offers a substantial improvement in electronic properties (compared to no oxide) with a relatively small reduction in optical performance.

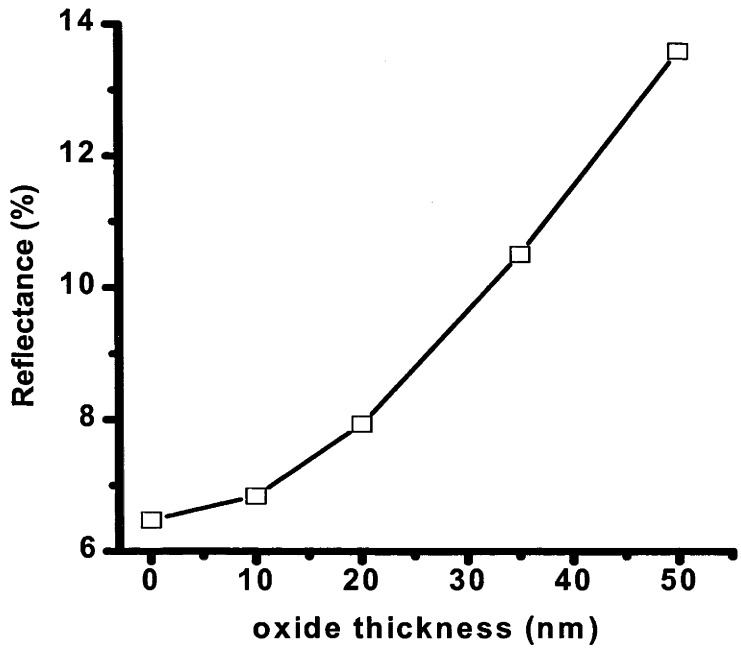

Figure 3.47. The modelled dependence of the reflectance of planar wafers featuring an Si_3N_4/SiO_2 coating encapsulated behind glass, as a function of oxide thickness. The nitride thickness has been optimised for each data point to obtain the lowest reflectance.

3.6 H reintroduction by FGA to Si-SiO_2 interface properties

Hydrogen reintroduction into Si_3N_4 films by annealing in forming gas at high temperatures was discussed in section 3.2. In this section, the influence of this hydrogen reintroduction process on Si-SiO_2 interface passivation is studied in detail. FZ, (100) and (111) oriented, high resistivity ($\geq$ 100 Ω-cm), 500 μm thick wafers were initially etched in 10:1 HNO_3:HF solution until shiny. Both sides of the wafers first received a light phosphorus diffusion (with a sheet resistance R_{sh} of ~400 Ω/□ after thermal drive in), followed by the growth of an 80 nm thick thermal oxide, a 30 minute in situ anneal at 1000°C in nitrogen and a 30 minute anneal at 400°C in forming gas (5% H_2 / 95% Ar). This final anneal will hereafter be referred to as a low temperature FGA (LTFGA). Selected wafers then had 50 nm thick LPCVD silicon nitride deposited on both sides. All depositions were done at 775°C, a pressure of 0.5 torr and ammonia to dichlorosilane (DCS) gas flow ratio of 5 to 1.

Figure 3.48 shows the change in J_{oe} as silicon samples are taken through various processing steps. For these experiments the thicknesses of the oxide and nitride films were 80 nm and 50 nm, respectively. (100) and (111) Si surfaces were compared. Three samples were used for the average values after each step. Just after nitride deposition, the surfaces are well passivated with

a low value of J_{oe}. The nitrogen anneal results in a substantial increase in J_{oe}, chiefly as a result of a loss of hydrogen from the Si-SiO_2 interface where the hydrogen passivates interface defects. The subsequent high temperature, 840°C FGAs result in a gradual re-passivation of the interface, indicating that hydrogen has diffused through the nitride and oxide films and has bonded with interfacial defects despite the relatively high anneal temperature. Diffusion of hydrogen through the oxide layer at such a high temperature will be extremely rapid, so that the presence of the oxide does not present a significant additional barrier to the diffusion of hydrogen to the silicon surface.

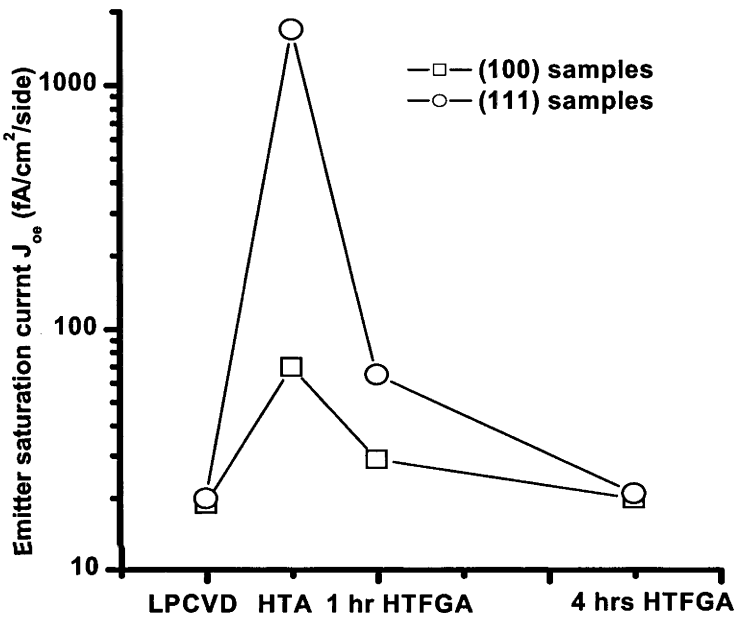

Figure 3.48. Emitter saturation current density Joe for (111) and (100) Si orientation in $Si_3N_4/SiO_2/Si$ stacks. 'LPCVD' means just after LPCVD deposition. 'HTA' means annealing in nitrogen at 900°C for 30 minutes. '1hr HTFGA' represents a subsequent annealing in forming gas at 840°C for 1hour and '4 hrs HTFGA' means annealing in forming gas at 840°C for 4 hours.

Both (100) and (111) samples follow a very similar trend. However, (111) surfaces exhibit higher J_{oe} values at each stage and a much faster de-passivation rate during the N_2 anneal, probably due to a higher concentration of (electrically active) defects at (111) compared to (100) Si-SiO_2 interfaces prepared under similar conditions. The results of Stesmans [77] indicate post oxidation vacuum anneals above 640°C result in about 2 times more paramagnetic defects at (111) than (100) Si-SiO_2 interfaces.

A plausible explanation of the results of the FTIR and photoconductance decay measurements is that the hydrogen for re-passivation of the interfacial defects is supplied chiefly by atomic hydrogen created by the breaking of Si-H and N-H bonds. A qualitative

description for the process is as follows. The rate of generation of atomic hydrogen would be expected to increase with increasing concentration of bonded hydrogen. Once atomic hydrogen is liberated, it will diffuse with a certain mean path length prior to re-bonding in the nitride film. Atomic hydrogen in the vicinity of the SiO_2 layer may also diffuse across the SiO_2 layer and passivate defects at the $Si\text{-}SiO_2$ interface. Thus, the degree of interface passivation would be expected to improve with increasing concentration of bonded hydrogen in the nitride film.

The conclusion that the bonded hydrogen in the nitride film can play a key role in $Si\text{-}SiO_2$ interface passivation is consistent with the results of McCann et al.[106], who showed that the degradation in J_{oe} of Si/SiO_2/LPCVD Si_3N_4 stacks during high temperature nitrogen anneals decreased substantially as the nitride layer thickness was increased, due to an increased supply of atomic hydrogen from hydrogen bonds in the nitride layer.

The fact that $Si\text{-}SiO_2$ interfaces can effectively be re-passivated at a temperature as high as 840°C is remarkable. Stesmans[74], studying the de-passivation of the dominant P_b centre defect on (111) silicon, showed that this defect is virtually entirely de-passivated after a 1 hour vacuum anneal at a temperature of only 650°C. Calculations using the model developed by Stesmans also indicate that a 1 hour anneal in pure H_2 at 840°C may still result in the passivation of around 99.9% of all P_b centres, for a good quality $Si\text{-}SiO_2$ interface[76]. However, in the case studied here the supply of hydrogen to the interface is likely to be orders of magnitude lower, so that the same efficiency of passivation would not be expected. It is possible that the passivation process is more accurately described as a two step process, where the first step is the re-hydrogenation of the nitride film at a high temperature, and the second step, namely the effective passivation of interface defects, may occur at intermediate temperatures as the sample cools to room temperature. If the latter description is more appropriate, one may expect the rate of cooling of the samples to have a significant effect on the measured value of J_{oe}. However, experiments with different cooling rates (one, a rapid cool in which the samples were removed and cooled to <100°C within ten seconds and the other a slow cool in which the samples were ramped down to <100°C in 10 minutes) have not revealed significant differences in J_{oe}.

A further interesting observation relates to hydrogen-induced defect creation at the $Si\text{-}SiO_2$ interface. Stesmans showed that extended high temperature (> 700°C) hydrogen anneals lead to a marked generation of P_b centres on (111) surfaces[77], which he detected after vacuum annealing by electron paramagnetic resonance (EPR). At a temperature of 800°C, hydrogen annealing led to a 6-fold increase in P_b centre density. This increase in defect density is also hinted at by an increase in the value of J_{oe}. Figure 3.49 compares the values of J_{oe} for Si/SiO_2 stacks at various stages of processing. These samples were first oxidized and passivated with an LTFGA. This was followed by a 30 min 900°C nitrogen anneal and a 1hr 840°C, HTFGA. The stacks then received a second LTFGA. Finally, the oxide was stripped and regrown, and the stacks were again re-passivated using another LTFGA. The value of J_{oe} can be seen to be higher for the Si/SiO_2 stacks just after the HTFGA. The fact that the subsequent low temperature FGA

did not reduce J_{oe} to near its initial value can be attributed to the generation of additional defects as a result of the high temperature FGA, resulting in a greater density of residual (unpassivated) defects following the LTFGA. Only re-oxidation reduces the defect density, and the value of J_{oe}, back to near its initial value, in agreement with the results of EPR measurements [72].

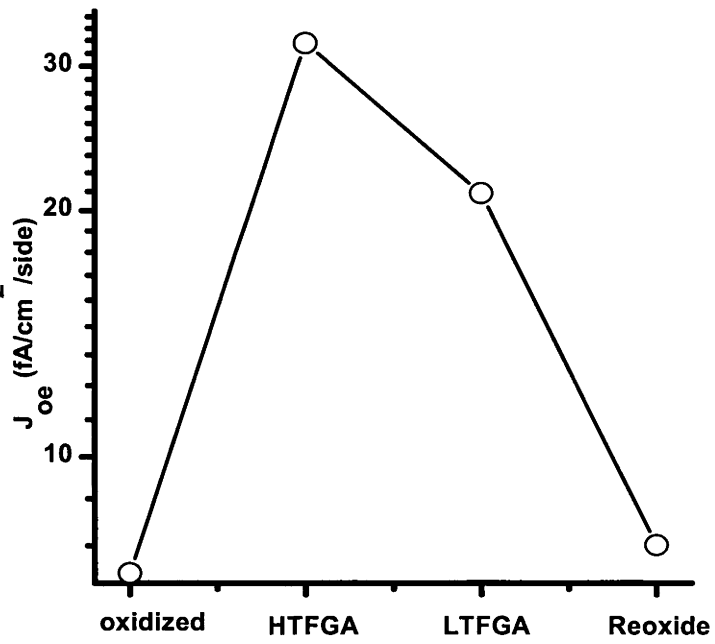

Figure 3.49. Emitter saturation current density (J_{oe}) values (fA/cm^2/side) of (100) silicon samples measured after various process steps - initial oxidation and LTFGA (LTFGA); 1 hour, 840°C high temperature FGA (HTFGA); a subsequent LTFGA; and re-oxidation and LTFGA. Every value is the average of three samples.

Thus, it is clear that care needs to be exercised when employing high temperature hydrogen anneals. There are two possible explanations for the better passivation observed following high temperature FGAs when a nitride layer is present. Firstly, the amount of hydrogen reaching the interface in the presence of a nitride layer is much less than in the case where only an oxide is present, so that the rate of generation of additional defects may be much lower. Secondly, it is possible that the atomic hydrogen supplied by the nitride layer provides much more efficient interface passivation than the molecular hydrogen for the case where only an oxide is present. It is well known that much lower values of J_{oe} can be achieved following the FGA of oxides if a thin layer of aluminium is deposited on the oxide prior to annealing. Such 'alneals' are believed to be more efficient at interface passivation as a result of the generation of atomic hydrogen at the aluminium-oxide interface. However, it should be mentioned that in experiments using atomic hydrogen for Si-SiO2 interface passivation, to be presented in the next chapter, interface passivation has been consistently worse than that achieved with an LTFGA.

3.7 Phosphorus diffusion influence on Si surface passivation in $Si_3N_4/SiO_2/Si$ stacks

As discussed in section 2.4.2, phosphorus may influence the Si-SiO_2 interface recombination velocity. However, lifetime-voltage measurements on SiO_2/Si structures suffered from large leakage currents. These leakage currents introduce potential drops across the surface of the sample and/or at the Si-metal contact, and make such measurements difficult to interpret. The use of SiO_2 / LPCVD Si_3N_4 stacks resulted in much lower leakage currents and thus overcame this problem.

Samples used for lifetime-voltage measurements are p type, float zone, (100), >100 Ωcm, 500 μm thick Si wafers. After etching in acid solution and a standard RCA cleaning, selected samples received light phosphorus diffusion (~300-400 Ω/□ after thermal drive in). An oxide around 50 nm was thermally grown at 1000°C in dry oxygen on both sides of all samples with an in-situ anneal in nitrogen, followed by annealing in forming gas (FGA, 5% H2 in 95% Ar gas) at 400°C for 30 min. ~50 nm thick LPCVD Si_3N_4 was deposited at 775°C and 0.5 torr on both side of the oxidized sample. ~5 nm Al was thermally evaporated on both sides of all samples. HF solution was used to open the window for Si bulk connecting. Bulk contact was realized by GaIn paste.

Figures 3.50 and 3.51 show the effective lifetime and J_{oe} values for $Si_3N_4/SiO_2/Si$ structures from the lifetime-voltage measurement. The difference in Joe between diffused and undiffused samples will be partly due to emitter recombination in the diffused samples. In fact, modeling suggests that the small difference in J_{oe} for the oxide only samples in section 2.4.2 can be explained on the basis of the additional contribution of the emitter alone (~2 fA/cm2/side). However, the slightly larger difference for the oxide/nitride samples (4-5 fA/cm2/side) in both accumulation and inversion indicates a possible increase in the interface defect density, consistent with the results of Snel[72].

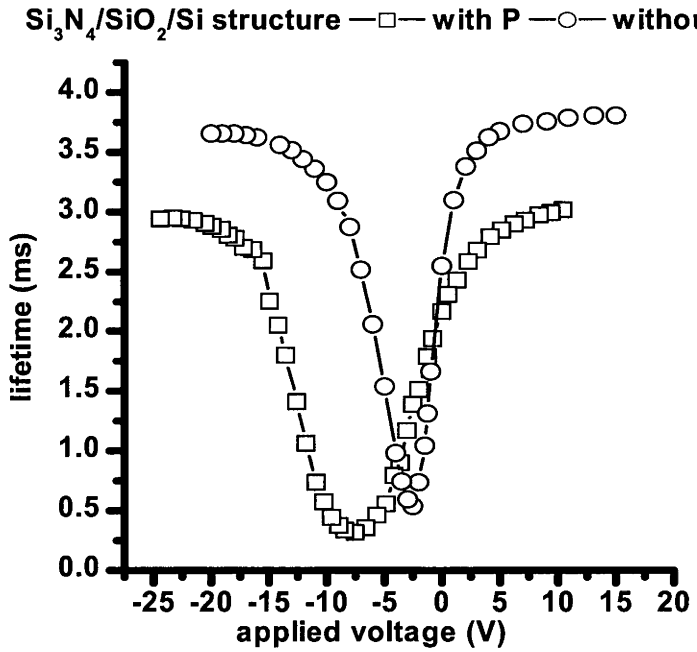

Figure 3.50. lifetime vs applied voltage for $Si_3N_4/SiO_2/Si$ structure. The sheet resistance is around 400 Ω/□ for the P diffused sample

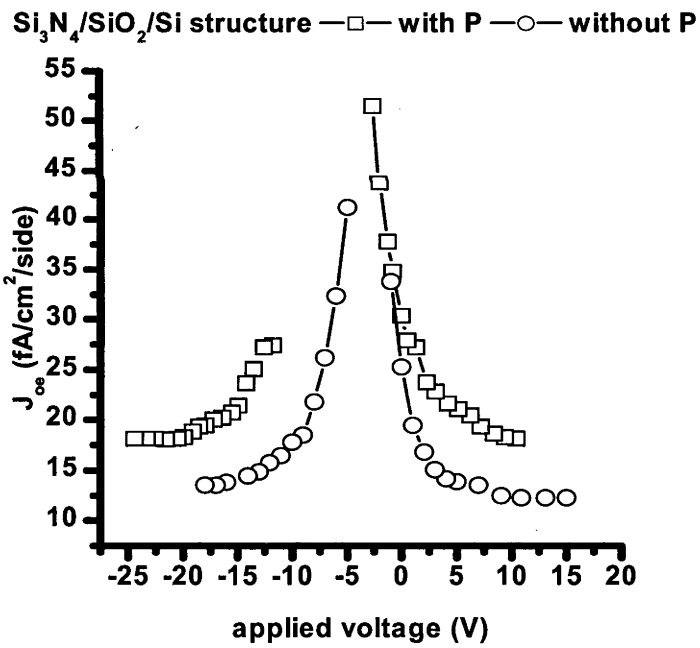

Figure 3.51 J_{oe} vs applied voltage for $Si_3N_4/SiO_2/Si$ structure. The sheet resistance is around 400 Ω/□ for the P diffused sample

Table 3.12 shows the effective surface recombination velocity in accumulation and inversion for nitride/oxide structures.

	S_{eff} in accumulation		S_{eff} in inversion	
	With P	Without P	With P	Without P
$Si_3N_4/SiO_2/Si$	4.8	3.5	4.8	3.2

Table 3.12 Effective surface recombination velocity from accumulation and inversion for $Si_3N_4/SiO_2/Si$ and SiO_2/Si structures

3.8 Summary

In summary, LPCVD Si_3N_4 is a potentially useful material for solar cells. It is a good diffusion and oxidation barrier, is resistant to chemical etching, can be mass-produced and provides a conformal coating. With an excess of ammonia, the nitride is nearly stoichiometric. It has low hydrogen content but can provide good surface passivation and anti-reflection properties together with an oxide layer.

The LPCVD Si_3N_4 layer contains a certain amount of charge, especially at the Si-Si_3N_4 interface. In addition, C-V curves of nitride layers deposited directly on Si display hysteresis, thought to be due to the charging and discharging of defects in the nitride bulk close to the interface. The charge density decreases with thermal annealing due to the removal of defects from the Si_3N_4 bulk. With an oxide between Si and Si_3N_4, the charge density in the nitride is reduced and the hysteresis effect disappears.

Direct deposition of Si_3N_4 on Si causes bulk and surface damage to Si wafers. However, with an oxide layer between Si and Si_3N_4, bulk damage is virtually eliminated and surface damage is significantly reduced. Nevertheless, Si_3N_4 deposition on an oxidised Si wafer influences the Si-SiO_2 interface properties by changing the interface defect properties and increasing the defect density, as shown by EPR and C-V measurements. The change of interface defect properties and density is accompanied by an increase of Si surface recombination velocity, shown by lifetime and lifetime-voltage measurements. The SiO_2/Si structure after LPCVD nitride deposition and removal shows a worse thermal stability than the as oxidized SiO_2/Si structure.

The Si-SiO_2 interface electronic properties of $Si_3N_4/SiO_2/Si$ stacks are influenced by the nitride deposition parameters. Among these parameters, the ammonia to DCS ratio appears to be the most important. The surface recombination velocity increases with increasing ammonia to DCS ratio.

The Si-SiO_2 interface electronic properties of $Si_3N_4/SiO_2/Si$ stacks also depend on the thickness of the SiO_2 layer. Both the surface recombination velocity and interface defect

density increase with decreasing oxide thickness. However, the recombination velocity shows little dependence on the nitride thickness for a nitride thickness greater than ~10 nm.

The role of hydrogen in LPCVD nitride films was studied in some detail. It was shown that the hydrogen concentration decreases significantly following high temperature (>= 900°C) treatments in a hydrogen free atmosphere, as a result of the breaking of Si-H and N-H bonds and the subsequent out-diffusion of hydrogen. FGA at high temperature (~840°C) can reintroduce hydrogen to the nitride layer and also passivate the $Si\text{-}SiO_2$ interface of $Si_3N_4/SiO_2/Si$ structures. In fact, with such high temperature FGAs it was possible to realise excellent surface passivation, indicating nearly complete hydrogenation of interface defects.

The Si_3N_4 films density following various thermal treatments was investigated qualitatively by measuring the film etch rate in HF solution. This indicated that higher temperature thermal anneals results in greater densification of the nitride film.

The thermal stability of $Si_3N_4/SiO_2/Si$ stacks was compared with that of SiO_2/Si structures. Is was shown that $Si_3N_4/SiO_2/Si$ stacks have a better thermal stability than the SiO_2/Si structures due to the gradual release of hydrogen from the nitride layer, which is able to passivate interface defects and thus partly compensates for hydrogen lost by interface defects during thermal treatments.

CHAPTER 4

The effect of exposure of SiO_2/Si and Si_3N_4/SiO_2/Si structures to atomic hydrogen

Hydrogen plays a critical role in passivating the Si-SiO_2 interface of SiO_2/Si and Si_3N_4/SiO_2/Si structures by bonding with defects, and thus rendering them electrically inactive. In order to passivate the interface defects in nitride coated stacks, hydrogen must be able to diffuse through the nitride film towards the Si-SiO_2 interface. In the last chapter H introduction was realized by exposing samples to molecular hydrogen at high temperatures (around 800°C to 900°C) for several hours. However, the long processing time and high thermal budget required mean this type of process is of limited interest for practical applications. In this chapter, ammonia is dissociated in a direct Plasma Enhanced Chemical Vapor Deposition (PECVD) chamber at

13.56 MHz. The plasma generated will contain atomic H, atomic N, NH, and other N-H species, which may be neutral or charged. The Si surface properties following ammonia plasma exposure are studied for SiO_2/Si and Si_3N_4/SiO_2/Si structures. A limited number of experiments are also carried out using remote plasma with molecular hydrogen as the source gas, and the results of the two different types of plasma are compared.

It is shown that ammonia plasma can be used to ensure the rapid diffusion of atomic hydrogen through LPCVD Si_3N_4 films, and the passivation of the interface of Si/SiO_2/Si_3N_4 stacks at comparatively low temperatures (400°C). Ammonia plasma exposure to SiO_2/Si structures also introduces nitrogen species into the SiO_2 layer and the Si-SiO_2 interface, forming an oxynitride interface.

4.1 Introduction

In this chapter, the effect of ammonia or hydrogen plasma exposure to SiO_2/Si and Si_3N_4/SiO_2/Si structures is studied. A chief motivation for this work is that such treatments offer the possibility to be able to re-hydrogenate Si-SiO_2 interfaces which may have been de-hydrogenated to some degree by the process of LPCVD nitride deposition, or subsequent thermal treatments. Both ammonia and hydrogen plasmas generate atomic hydrogen which can can be used for this purpose. In contrast to molecular hydrogen, atomic hydrogen diffuses readily through both oxide and nitride films at relatively low temperature, offering the possibility of avoiding the high temperature, prolonged treatments necessary with molecular hydrogen (described in Ch3).

4.2 Ammonia plasma exposure of SiO_2/Si structures at 400°C

4.2.1 Experimental Method

NH_3 plasma exposure is realized by operating an Oxford Plasmalab 80+ direct PECVD using system. A schematic diagram of the system is shown in figure 4.1.

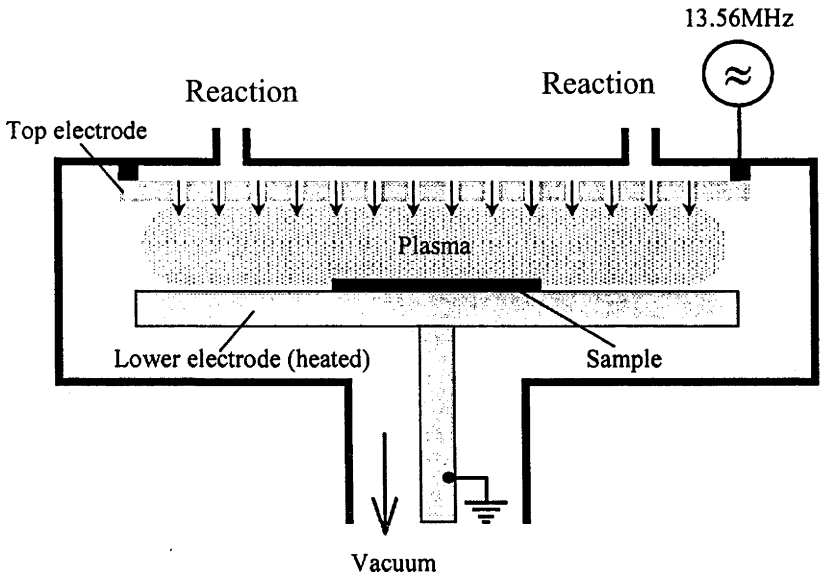

Figure 4.1. A schematic diagram of the plasma system

The substrate is placed on a heated lower electrode. The chamber is then closed and evacuated to a pressure of around 10 mTorr. The processing gas is injected into the reactor at the desired flow rates. A constant pressure is maintained inside the chamber by pumping out gases. An oscillating RF field is applied between the upper and lower electrode to generate the plasma. A high excitation frequency (13.56 MHz) is used to minimize the plasma damage. In our experiments, the system operates with only ammonia at 400°C and an RF power ranging from 5 W to 200 W at a pressure of 0.5 torr. At the end of the exposure, the plasma and the ammonia are turned off, and the chamber is evacuated. The samples were still heated with heater on at 400°C for about half a minute during the evacuation. Lifetime measurements were used for characterizing the Si surface recombination velocity. C-V and EPR measurements were applied for quantifying the Si surface defect density.

FZ, p-type, >100 Ω-cm, (100), as cut Si wafers were used as the starting material for lifetime measurements. After acid etching and standard RCA clean, the wafers were given a light phosphorus diffusion (R~ 300-400 Ω/□ after thermal drive in), and passivated with a thermally grown 50 nm oxide at 1000°C, followed by in-situ anneal in N_2 at the same temperature for 30 minutes. Annealing in forming gas (FGA, 5% H_2 in 95%Ar) at 400°C was performed on selected samples to hydrogenate the Si-SiO_2 interface. RTA treatments were performed at 800°C for 3 minutes in N_2 flow on selected samples to de-hydrogenate Si-SiO_2 interface[101].

Cz, p-type, 10-23 Ω-cm, (100), single side polished wafers were used for C-V measurements and Secondary Ion Mass Spectroscopy (SIMS) profiling. For C-V measurements, after etching in acid solution to remove surface damage, ~100 nm thick SiO_2 layers were

thermally grown in dry oxygen at 1000°C on Si, followed by an in-situ anneal in N_2 at the oxidation temperature for 30 minutes. An FGA was carried out at 400°C for 30 minutes to hydrogenate the Si-SiO_2 interface. For SIMS, ~100 nm oxide layers were thermally grown without in-situ nitrogen anneal before plasma exposure.

Cz, p-type, ~10 Ω-cm, (111) silicon wafers in 25 mm×2.5 mm pieces were used for EPR measurements. Surface damage was removed by etching in HNO_3:HF solution. A 50 nm thick oxide layer was thermally grown at 1000°C, followed by an in-situ anneal in N_2 for 30 minutes at the same temperature and a 400°C FGA for 30 minutes.

4.2.2 Nitrogen introduction into the SiO_2 layer and to the Si-SiO_2 interface

The nitrogen distribution in the oxide following ammonia plasma exposure was analysed by SIMS, shown in figure 4.2. The plasma NH_3 exposure was carried out at 400°C and 200 W for 20 minutes. The nitrogen concentration is relatively high in the SiO_2 surface region and decreases toward the interface. A sharp peak can be observed at the Si-SiO_2 interface. Thus, ammonia plasma exposure under the conditions used here leads to nitrogen introduction chiefly in the SiO_2 surface and Si- SiO_2 interface regions. It is hypothesized that atomic N in neutral or (+/-) charged forms pass through the oxide layer and react with Si interface. The possible charged atoms was identified to be more responsible to the reaction[126].

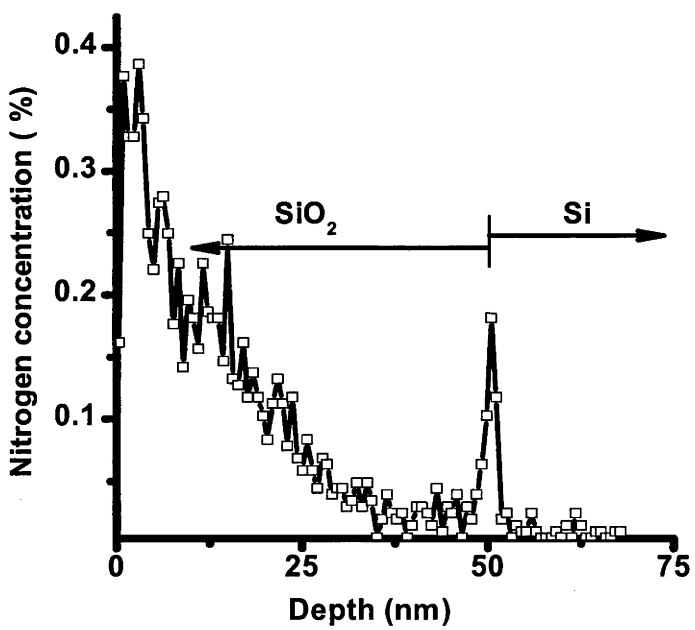

Figure 4.2. Depth profile of the nitrogen concentration in SiO_2/Si stacks after plasma NH_3 exposure at 400°C for 20 minutes

4.2.3 Influence of ammonia plasma exposure on the Si-SiO_2 interface

Ammonia plasma exposure of SiO_2/Si stacks introduces nitrogen to the Si-SiO_2 interface and the SiO_2 bulk. In this section, the Si-SiO_2 interface properties after ammonia plasma exposure are discussed and compared with the as grown Si-SiO_2 interface.

4.2.3.1 Influence of ammonia plasma exposure on Si surface recombination

Figure 4.3 shows J_{oe} values for SiO_2/Si stacks measured after plasma NH_3 exposure at an RF power ranging from 5 W to 200 W for 5 minutes. The circle symbols represent results from initially hydrogenated Si-SiO_2 interfaces (realized by an RTA in N_2 at 800°C for 3 minutes). The rectangle symbols represent results from initially dehydrogenated Si-SiO_2 interfaces (realized by FGA in forming gas at 400°C for 30 minutes). The J_{oe} values at zero exposure time come from samples that did not receive any plasma exposure.

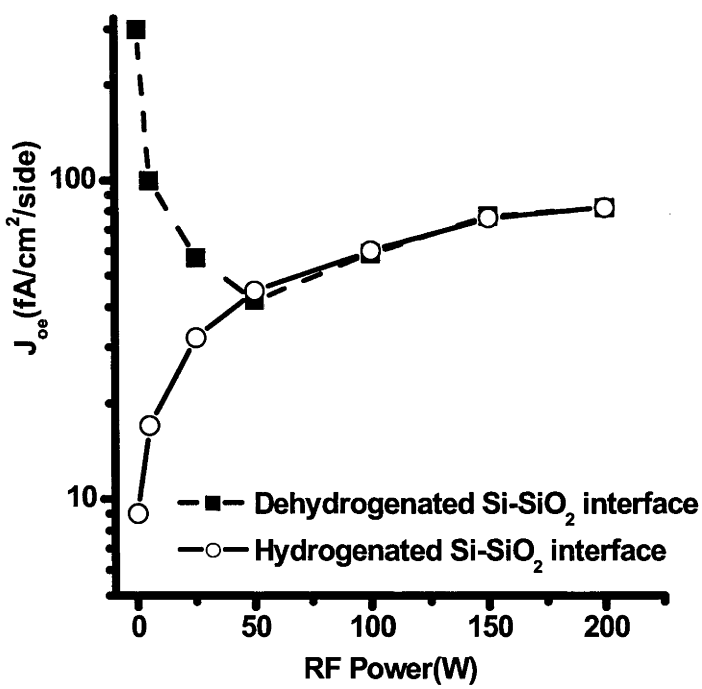

Figure 4.3 J_{oe} for hydrogenated and dehydrogenated SiO_2/Si structures after ammonia plasma exposure at an RF power ranging from 5 to 200 W for 5 minutes

At relatively low power levels (<50 W), a 5 minute ammonia plasma exposure passivates the dehydrogenated Si-SiO_2 interface and de-passivates the hydrogenated Si-SiO_2 interface. At exposure powers of 50 W or higher, exposure results in nearly the same J_{oe} values for both an initially hydrogenated and dehydrogenated interface. At the highest power levels used, J_{oe} saturates.

At the process pressure used for the experiments, molecular hydrogen has little influence on Si-SiO_2 interface passivation[127]. Atomic H is known to be able to passivate and de-passivate the Si-SiO_2 interface at the same time, with reactions (4.1) and (4.2) taking place simultaneously[55].

$$D+H \rightarrow DH \qquad (4.1)$$

$$DH \rightarrow D+H \qquad (4.2)$$

where D represents an interface defect. The passivation effect to the initially dehydrogenated Si-SiO_2 interface is considered to result from the bonding of defects with atomic H, as shown in equation 4.1 while the de-passivation effect to the initially hydrogenated Si-SiO_2 interface is considered to be partly the result of the dissociation of D-H bonds. For an RF power level of 50 W or more, the interface reaches steady state conditions within less than 5 minutes, so that the initial state of the Si-SiO_2 interface (passivated or de-passivated) is no longer of significance.

As discussed in the previous chapter, nitridation of the SiO_2 layer and the interface may degrade the interface properties and increase the Si surface recombination velocity. The increase of the J_{oe} values in figure 4.3 with increasing RF power is likely to be at least partly due to nitridation effects.

Figure 4.4 shows J_{oe} values for SiO_2/Si stacks measured after plasma NH_3 exposure at an RF power of 200 W for 2.5 to 20 minutes. The circle symbols represent results from an initially dehydrogenated Si-SiO_2 interface (realized by RTA in N_2 at 800°C for 3 minutes). The rectangle symbols represent results from an initially hydrogenated Si-SiO_2 interface (realized by FGA in forming gas at 400°C for 30 minutes). Values at zero reaction time come from samples prior to plasma exposure. For this RF power, steady state conditions are reached after only 2.5 minutes of exposure. The increase of J_{oe} for longer exposure times indicates a gradual degradation of the interface, which can be at least partly attributed to nitridation effects.

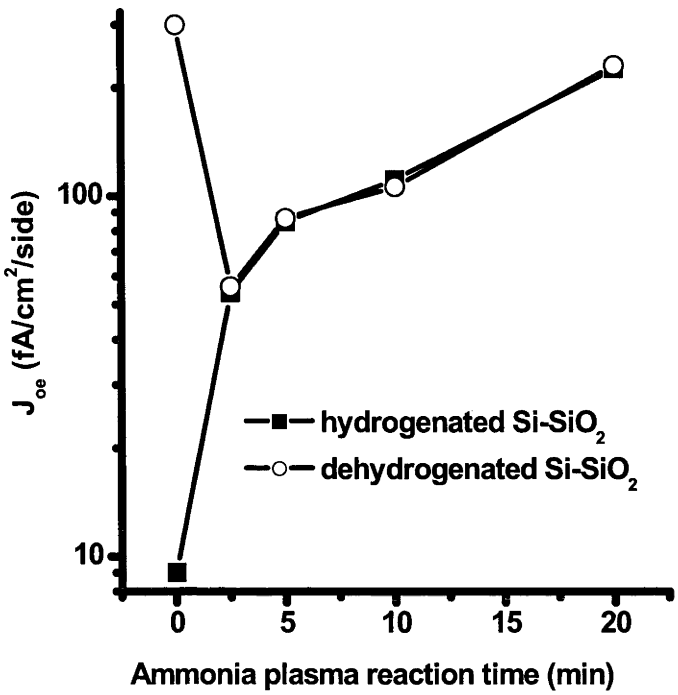

Figure 4.4 J_{oe} for initially hydrogenated and de-hydrogenated SiO_2/Si structures after ammonia plasma exposure at 200 W for 2.5 to 20 minutes.

4.2.3.2 Influence of a post ammonia plasma exposure forming gas anneal on Si surface recombination

Forming gas annealing after ammonia plasma exposure was carried out to re-hydrogenate the Si-SiO_2 interface. Figure 4.5 shows the J_{oe} values measured after ammonia plasma exposure at RF powers from 5 to 200 W for 5 minutes and a subsequent FGA at 400°C for 30 minutes.

Figure 4.5 clearly reveals the evolution of interface damage with RF exposure power, by removing the competing effects of hydrogenation and de-hydrogenation arising from the action of atomic hydrogen. Initially hydrogenated and dehydrogenated interfaces now have nearly the same J_{oe} values at all power levels, depending only on the plasma exposure power. With increasing RF power, interface damage increases and appears to saturate at around 200 W. Figure 4.6 shows J_{oe} for hydrogenated and dehydrogenated SiO_2/Si structures after ammonia plasma exposure at 200 W for 2.5 to 20 minutes and a subsequent FGA at 400°C for 20 minutes

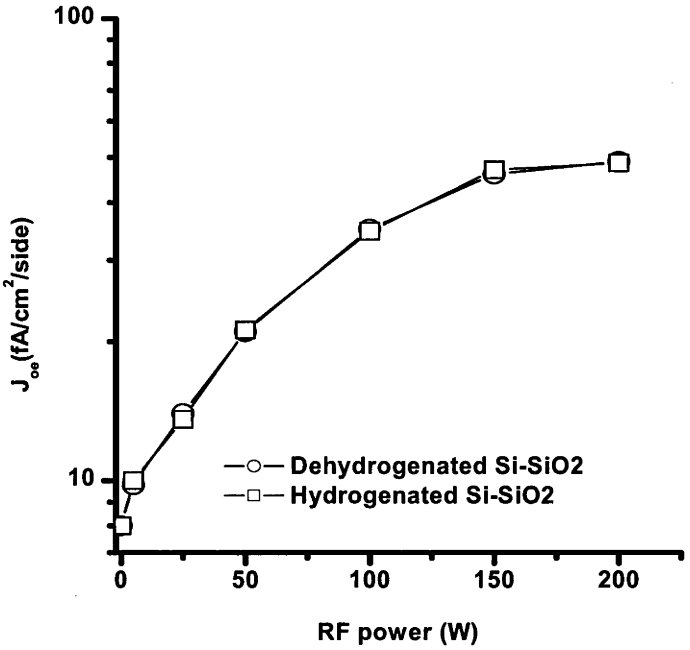

Figure 4.5 J_{oe} for hydrogenated and dehydrogenated SiO_2/Si structures after ammonia plasma exposure at 5 to 200 W for 5 minutes and a subsequent FGA at 400°C for 30 minutes

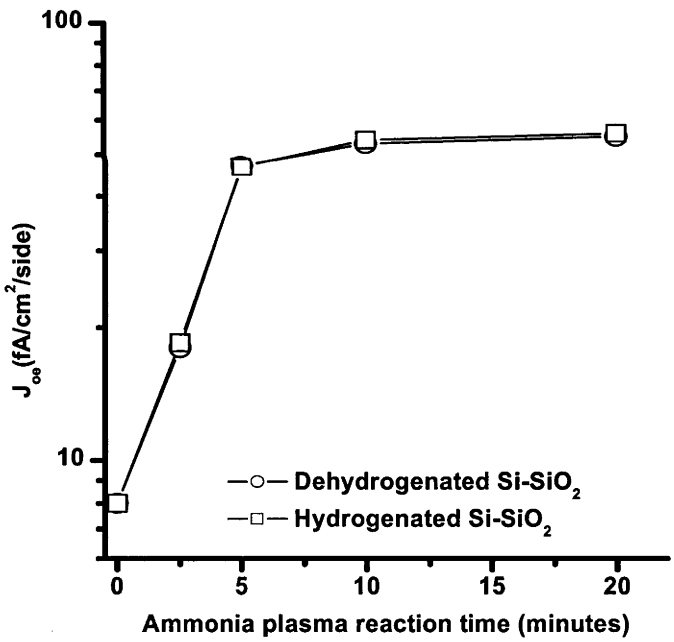

Figure 4.6 J_{oe} for hydrogenated and dehydrogenated SiO_2/Si structures after ammonia plasma exposure at power of 200 W for 2.5 to 20 minutes and a subsequent FGA at 400°C for 30 minutes

Similar to figure 4.5, the initially hydrogenated and dehydrogenated interfaces have nearly the same J_{oe} values, depending only on the plasma exposure time. Longer exposure time results in greater interface damage, with the damage saturating after an exposure time of ~10 minutes.

4.2.3.3 Defect generation at the Si-SiO_2 interface by ammonia plasma exposure

C-V and EPR measurements were carried out to study the Si-SiO_2 interface after ammonia plasma exposure. Figure 4.7 shows C-V curves for p type MOS stacks measured after i) FGA, ii) a subsequent plasma NH_3 exposure at 200 W for 5 minutes and iii) a subsequent FGA, with effective interface charge densities of 2.4×10^{11} cm^{-2}, 5.4×10^{11} cm^{-2} and 3.9×10^{11} cm^{-2}, respectively.

The mid gap defect density is 7.9×10^{9} $eV^{-1}cm^{-2}$ for FGAed stacks. It increases to 3.0×10^{11} $eV^{-1}cm^{-2}$ after plasma NH_3 exposure and decreases to 8.1×10^{10} $eV^{-1}cm^{-2}$ after a subsequent FGA. Thus, the C-V results indicate that plasma NH_3 exposure increases both the charge and interface defect density, while a subsequent FGA reduces them. However, the interface defect density of the hydrogenated post plasma exposure stacks is about 10 times of the hydrogenated as oxidized stacks, indicating additional defects have been generated by plasma NH_3 exposure.

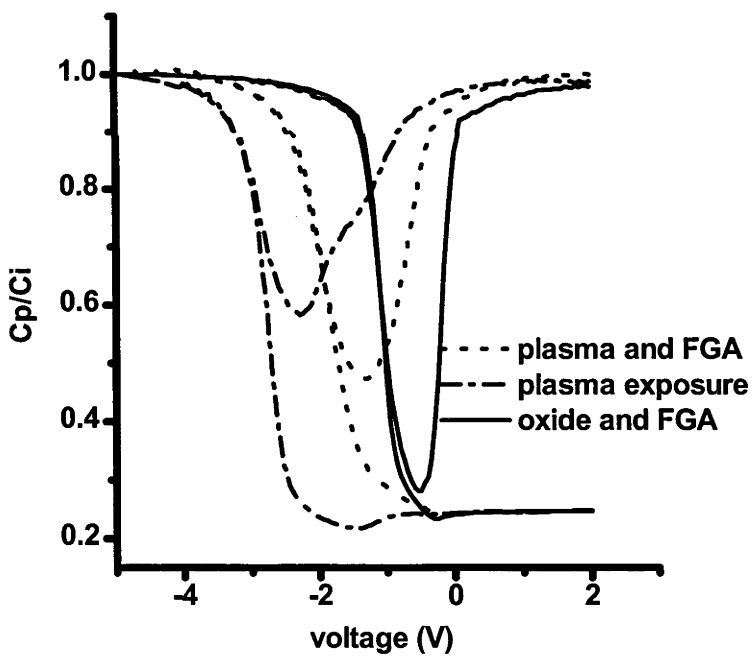

Figure 4.7. C-V curves for SiO_2/Si stacks after FGA, plasma NH_3 exposure and subsequent FGA

The effect of ammonia plasma exposure was also investigated using EPR. Figure 4.8 shows the spectra for an as oxidized sample and plasma ammonia treated sample with the magnetic field parallel to the (111) direction. Table 4.1 compares the g values and peak to peak linewidth ΔB_{pp}. An RTA at 800°C for 3 minutes was carried out before all measurements. The g value measured with the magnetic field parallel to the (111) direction decreases from the 'as oxidized'

value of 2.00141 to 2.00115 (with an error of ±0.00004). The peak to peak linewidth increases to 5.3G and 4.2G with the magnetic field is parallel and perpendicular to (111), respectively. The effect of the decrease of the g value and the broadening of linewidth is very similar to the change caused by the high temperature, thermal nitridation of the Si-SiO_2 interface using ammonia[119], where the changes were attributed to changes of the interface properties due to the introduction of nitrogen atoms to the interface.

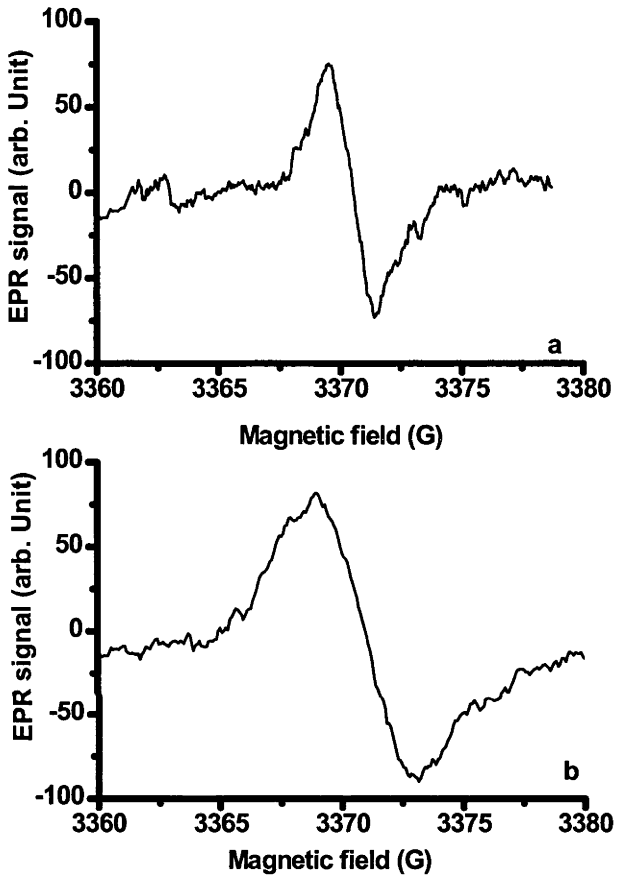

Figure 4.8 EPR spectra for (a) as oxidized and (b) oxidised and ammonia plasma exposed (5 minutes at 400°C for 5 minutes on both sides) samples. Both samples received a RTA at 800°C for 3 minutes in N_2 gas for 3 minutes before measurements. Both spectra were taken with the magnetic field set parallel to the (111) direction

	g//	ΔB_{pp}// (G)	g⊥	ΔBp_p⊥ (G)
No plasma treatment	2.00141	1.9	2.00860	3.8
With plasma treatment	2.00115	4.3	2.00864	5.3

Table 4.1 comparison of g value, peak to peak linewidth ΔB_{pp} and paramagnetic defect concentration of as oxidized and plasma treated samples. RTAs at 800°C for 3 minutes were carried out before measurements. '//' indicates magnetic field parallel to (111) direction, and '⊥' indicates magnetic field perpendicular to (111) direction. The error in the g value is 4×10^{-5}.

Figure 4.9 summarizes the interface paramagnetic defect density with plasma NH_3 exposure power. A RTA at 800°C for 3 minutes was conducted before measurement. At no plasma exposure, the spin density is around $4.2\times10^{12}/cm^2$. The density is much lower than the spin density measured after oxidation and dehydrogenation without insitu annealing in N_2, since in-situ annealing in N_2 significantly reduces the interface defect density. The dramatic increase of paramagnetic defect density indicates additional defects were generated by plasma NH_3 exposure.

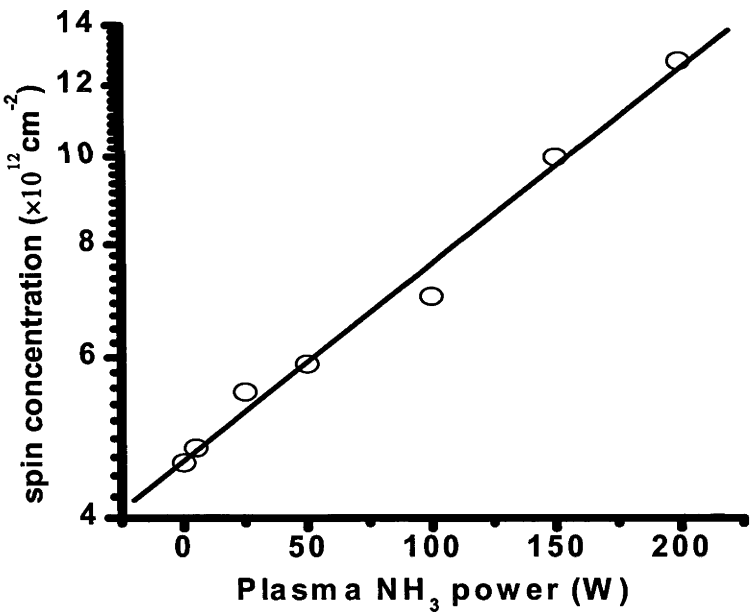

Figure 4.9. Paramagnetic defect density obtained by EPR measurement after plasma NH_3 exposure at an RF power ranging from 5 to 200 W for 5 minutes, followed by an RTA at 800°C for 3 minutes in N_2.

The improvement in surface passivation to an initially depassivated sample following short plasma exposure times (as shown in figures 4.3 and 4.4) is the result of the passivation of electrically active defects with atomic H[55]. However, atomic H does not cause an increase in the density of P_b centres or a change in their EPR signature, only a change in their bonding

state[55]. The observed increase in interface defect density and the change in the EPR signature may be due to the introduction of N atoms into the SiO_2 film, since N at the Si-SiO_2 interface generally causes an increasing rigidity[119] with the result that more dangling bonds are created to release the stress[68]. Another explanation is that the changes are due to radiation damage, as suggested by Dimitrova et al.[128]. These authors used plasma NH_3 exposure to SiO_2/Si stacks at around 370°C and noticed that charges and interface defects were created by the plasma exposure. This was attributed radiation damage. In contrast to our results, no interface nitridation was observed by these authors, probably because of the slight difference in experimental conditions.

4.2.3.4 Influence of ammonia plasma exposure on thermal stability

The thermal stability of SiO_2/Si structures following ammonia plasma exposure is studied and compared with as oxidized SiO_2/Si structures. RTAs were carried out at 800°C for 3 minutes and the J_{oe} values were measured. Figure 4.10 shows J_{oe} for hydrogenated and dehydrogenated SiO_2/Si structures after ammonia plasma exposure at powers ranging from 5 to 200 W for 5 minutes and a subsequent RTA.

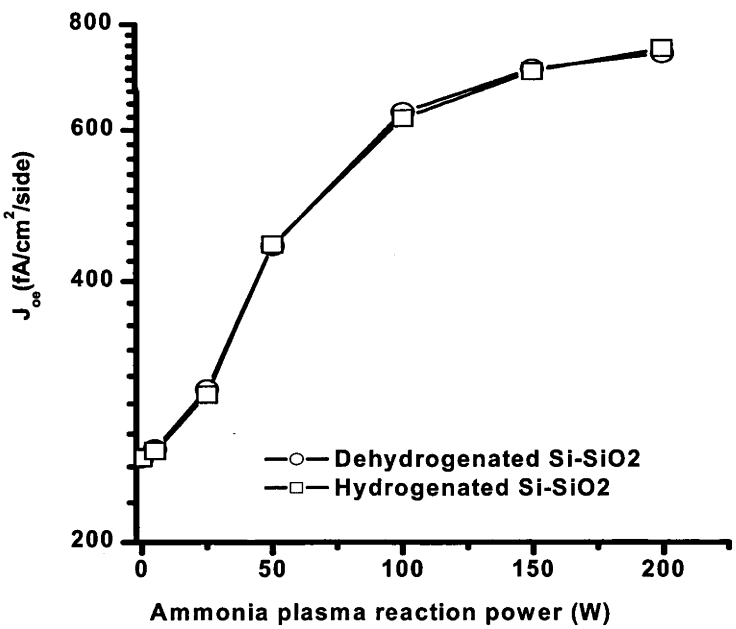

Figure 4.10 J_{oe} for initially hydrogenated and dehydrogenated SiO_2/Si structures after ammonia plasma exposure at RF powers ranging from 5 to 200 W for 5 minutes and a subsequent RTA at 800°C for 3 minutes

Comparing with figure 4.5, the J_{oe} values following ammonia plasma exposure and RTA have a similar trend to the J_{oe} values after ammonia plasma exposure and FGA, for both initially

hydrogenated and dehydrogenated interfaces. Initially hydrogenated and dehydrogenated interfaces have the nearly same J_{oe} values, depending only on the plasma exposure power. Figure 4.11 shows J_{oe} for initially hydrogenated and dehydrogenated SiO_2/Si structures after ammonia plasma exposure at 200 W for 2.5 to 20 minutes and a subsequent RTA.

Again, comparing with figure 4.6, J_{oe} values after ammonia plasma exposure and RTA have a similar trend with exposure time to the J_{oe} values after ammonia plasma exposure and FGA, for both initially hydrogenated and dehydrogenated interfaces, indicating degradation of thermal stability due to the ammonia plasma exposure.

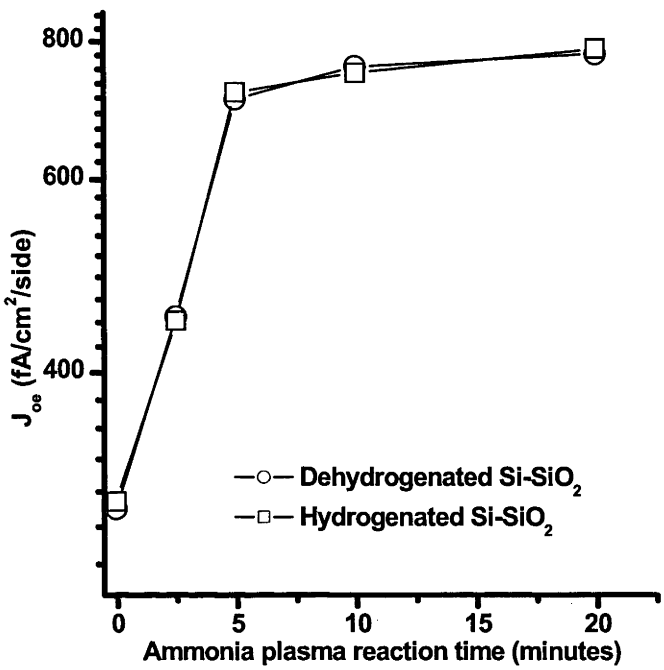

Figure 4.11. J_{oe} for initially hydrogenated and dehydrogenated SiO_2/Si structures after ammonia plasma exposure at power of 200 W for 2.5 to 20 minutes and a subsequent RTA at 800°C for 3 minutes

4.2.4 Comparison of direct ammonia plasma and remote hydrogen plasma exposure of the SiO_2/Si interface

In this section, a comparison is made between direct ammonia plasma and remote hydrogen plasma exposure to SiO_2/Si structures. A remote plasma system was used with pure H_2 gas in order to obtain atomic H. A brief description of the experiments is as follows.

The system used was a Microwave induced remote hydrogen plasma (MIRHP) system at the University of Konstanz. For the experiments, samples were placed in the slots of a quartz boat. The boat was then loaded inside the process quartz tube and the tube was

heated to the desired temperature and evacuated. The plasma reaction products were then admitted to the chamber. Following plasma exposure for the desired period of time, the plasma, was turned off, and the system was evacuated for 1-2 minutes and flushed with N_2. During this time, the samples remained at the process temperature. The time interval between turning off the plasma and ventilating the chamber was around 2 min. When the chamber was at atmospheric pressure, the chamber door was opened and the samples pulled out and allowed to cool. The system was operated at 400°C and 0.5 torr. Both atomic and molecular hydrogen will be present in the vicinity of the sample, since the plasma does not result in complete dissociation of the H_2 gas, and since the atomic H recombines rapidly in the chamber as soon as it is formed. However, molecular hydrogen has been shown to have little influence on the Si-SiO_2 interface at the operating pressure and temperature used here[127]. Thus, any changes in interface passivation can be ascribed to the action of the atomic hydrogen, or effects related to the presence of atomic hydrogen.

Figure 4.12 compares the influence of ammonia plasma and H_2 plasma exposure on the Si-SiO_2 interface. Initially hydrogenated and dehydrogenated SiO_2/Si structures were used and their J_{oe} values are shown at step 1.

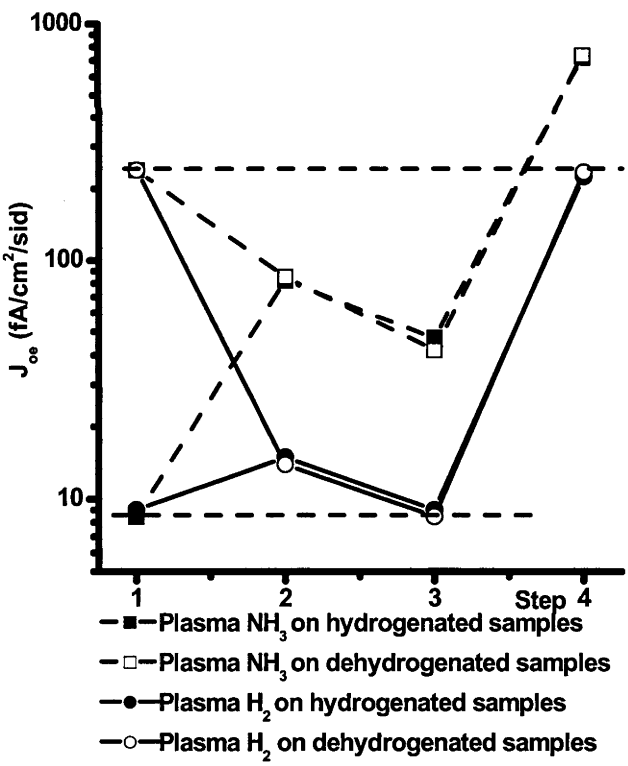

Figure 4.12. Comparison of the effect of plasma H_2 and NH_3 exposures on the Si-SiO_2 interface. Step 1: Oxidation and FGA or RTA Step 2: Plasma H_2 or NH_3 treatment Step 3: FGA at 400°C Step 4: RTA at 800°C for 3 minutes in N_2

At step 2, plasma H_2 and NH_3 exposure were carried out for 5 minutes. The surface passivation after plasma NH_3 exposure is much worse than after plasma H_2 exposure. At step 3, the FGA reduces the J_{oe} of the plasma H_2 samples back to the 'as oxidized and FGA' level while the J_{oe} values for the plasma NH_3 samples are about 4 times higher. At step 4, the RTA increases the J_{oe} of the plasma H_2 samples to the 'as oxidized and RTA' level while the J_{oe} values for plasma NH_3 samples are also about 4 times higher. The results show that there is a significant difference in the effect of direct ammonia plasma exposure and remote hydrogen plasma exposure. This will be discussed in more detail later.

4.3 Ammonia plasma exposure of SiO_2/Si structures at room temperature

In this section, ammonia plasma exposure of SiO_2/Si structures at the temperatures below 400°C is investigated. Most attention is focused on the case of ammonia plasma exposure at room temperature (~25°C).

4.3.1 Experimental methods

Czochralski, p-type, 10-23 Ω-cm, (100), ~500 μm thick wafers were used as the starting material for C-V measurements. After etching in acid solution to remove surface damage, ~100 nm thick SiO_2 layers were thermally grown in dry oxygen at 1000°C, followed by an in-situ anneal in N_2 at the oxidation temperature for 30 minutes. The oxide thickness was carefully chosen to optimize signals for C-V measurements. Annealing in forming gas was carried out at 400°C for 30 minutes to hydrogenate the Si-SiO_2 interface.

Prior to C-V measurements, ~80 nm Aluminium was deposited with an area of around 4.7×10^{-3} cm^2 through a shadow mask on the oxide to form a metal-oxide-semiconductor (MOS) structure. HFCV measurements were carried out at 1 MHz and QSCV measurements were carried out with a sweep rate of 100 mV/s.

Float-zoned (FZ), p-type, 100 Ω-cm, (100), ~500 μm thick wafers were used as the starting material for lifetime measurements. These wafers were supplied acid etched. It should be noted that this material was different (from a later batch) from the samples used in the last section. The wafers were given a light phosphorus diffusion (R~ 300-400 Ω/□ after thermal drive in), and passivated with a thermally grown 50 nm oxide, followed by a N_2 in-situ anneal at 1000°C

for 30 minutes and a 400°C FGA. Minority carrier lifetime measurements were carried out as discussed in chapter 1.

Czochralski, p-type, ~10 Ω-cm, (111), ~500 μm thick silicon samples were used for EPR measurements. Samples were cut with a diamond saw into 25 mm×2.5 mm pieces. They were subsequently etched to remove saw damage from the surfaces. An oxide layer around 50 nm thick was thermally grown on both sides at 1000°C, followed by an in-situ anneal in N_2 at the oxidation temperature for 30 minutes and a 400°C FGA. On selected samples, an RTA was carried out at 800°C for 3 minutes in a high flow of nitrogen gas to de-passivate the Si-SiO_2 interface and active the paramagnetic defects. By double integrating of the signal and comparing with a standard signal, the paramagnetic defect density is calculated.

Ammonia plasma exposure was realized at room temperature (25°C) and elevated temperature up to 400°C with an RF power from 25 W to 200 W in a direct, high frequency (13.56 MHz) PECVD chamber.

4.3.2 Dependence of Si-SiO_2 interface properties on temperature during ammonia plasma exposure

Ammonia plasma exposure was carried out at an RF power of 200 W for 5 minutes at a temperature ranging from 25°C to 400°C. Figure 4.13 summaries the J_{oe} results. Initially hydrogenated and dehydrogenated Si-SiO_2 interfaces have nearly the same J_{oe} values after the plasma exposure. The J_{oe} value after 400°C plasma ammonia exposure is lower than the result shown in figure 4.3, probably due to the difference in the wafers used, as mentioned above. For clarity, the samples used in figure 4.3 come from 'as cut' Si material which was subsequently etched in the lab, while the starting material used in figs. 4.13 and 4.14 was supplied acid etched by the producer.

Surprisingly, a lower temperature ammonia plasma exposure results in a much higher J_{oe} value, indicating a very high interface defect density. An in depth analysis of this effect at room temperature is presented in the following sections. After the plasma exposure, RTA at 800°C for 3 minutes was carried out and J_{oe} values were taken. Figure 4.14 shows those J_{oe} values.

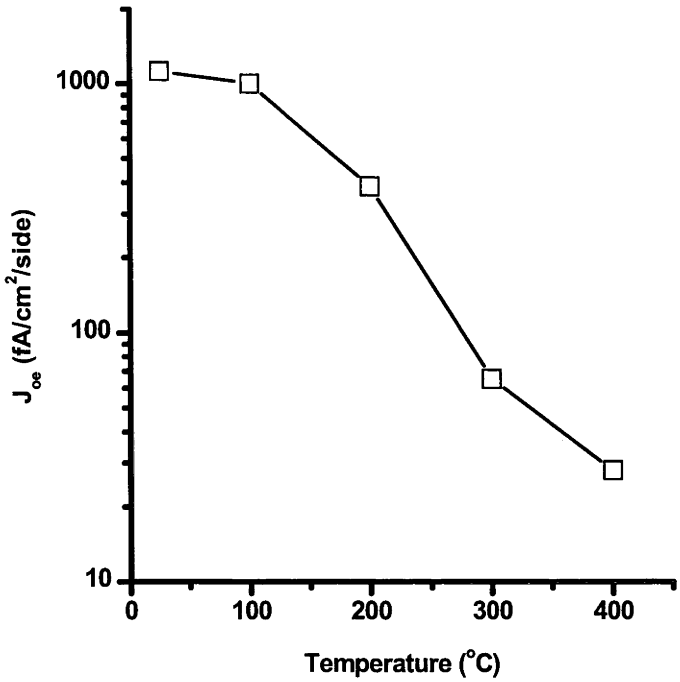

Figure 4.13. J_{oe} of SiO_2/Si stacks following ammonia plasma exposure at 25°C to 400°C for 5 minutes at 200 W.

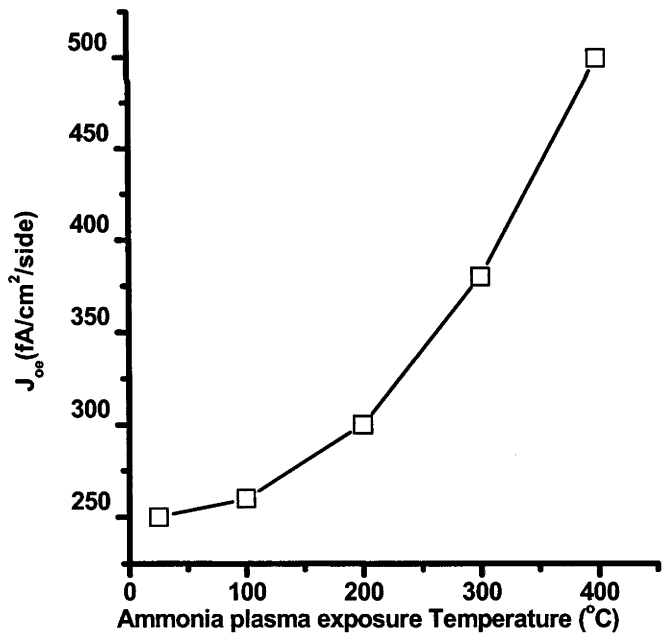

Figure 4.14. J_{oe} of SiO_2/Si stacks following ammonia plasma exposure at 25°C to 400°C for 5 minutes at 200 W, followed by a RTA at 800°C for 3 minutes.

The RTA in N_2 effectively reduces the J_{oe} values after room temperature ammonia plasma exposure. However, J_{oe} increases with the plasma exposure temperature.

4.3.3 Effect of ammonia plasma exposure at room temperature on Si interface properties

Figure 4.15 shows the HFCV and QSCV curves for p type MOS stacks prepared just after ammonia plasma exposure at room temperature and 200 W for 5 minutes. Before plasma treatment, the samples were hydrogenated (FGA at 400°C for 30 minutes). However, samples that were initially de-hydrogenated (RTA at 800°C for 3 minutes in N_2) gave nearly identical results following the same plasma treatment. The QSCV curve was taken sweeping from inversion to accumulation. The most striking feature in figure 4.15 is the high negative flat band voltage (-24.6 V for sweeping from inversion to accumulation and -27 V for sweeping from accumulation to inversion) and nearly flat QSCV curves. The effective (positive) net charge density is calculated to be $4.6\times10^{12}/cm^2$, in contrast to a density of about 2.5×10^{11} cm^{-2} for the same structure without the ammonia plasma treatment. The observed hysteresis of about +2.4 V is again attributed to the charging and discharging of interface defects via tunnelling of mobile holes, with a density of about $4.6\times10^{11}/cm^2$[117].

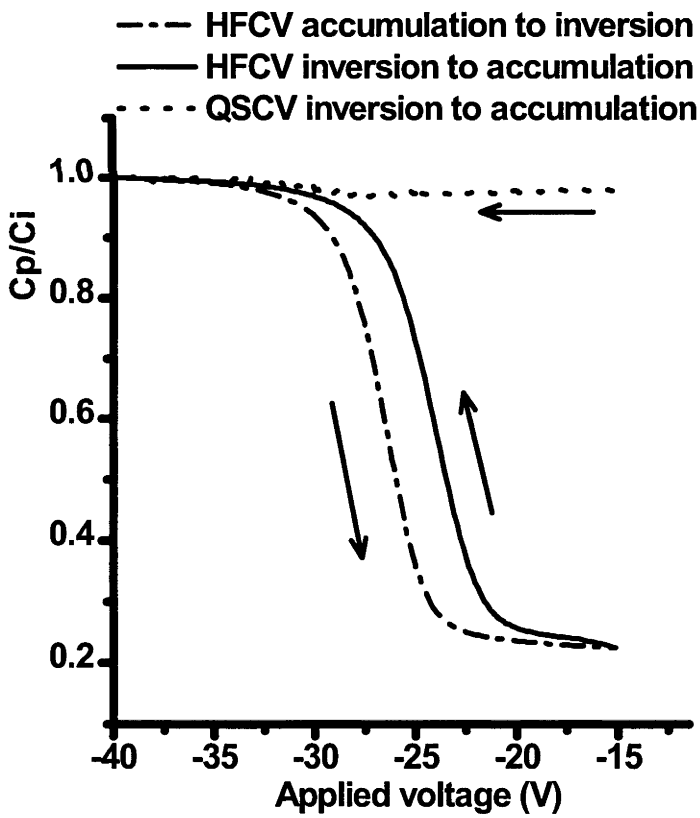

Figure 4.15. HFCV and QSCV curves for p-MOS stacks after 5 minute ammonia plasma treatment at 200 W. The sweeping directions are demonstrated by the arrows.

Usually, the QSCV curve shows a dip around the flat band voltage. The nearly flat QSCV response suggests a very high defect density at the Si-SiO_2 interface following plasma treatment[16]. However, an accurate quantitative determination of the defect density is not possible from these curves.

Figure 4.16 shows the dependence of J_{oe} on ammonia plasma power on both initially hydrogenated and de-hydrogenated samples. Ammonia plasma exposure was carried out at room temperature for 5 minutes with a plasma power ranging from 25 W to 200 W. Before plasma exposure, every hydrogenated sample had a J_{oe} value of around 6 fA/cm^2/side while for de-hydrogenated samples J_{oe} was around 160 fA/cm^2/side. The plasma exposure dramatically increases J_{oe}, again indicating that a large amount of interface defects were generated by the plasma treatment which caused an increase in surface recombination.

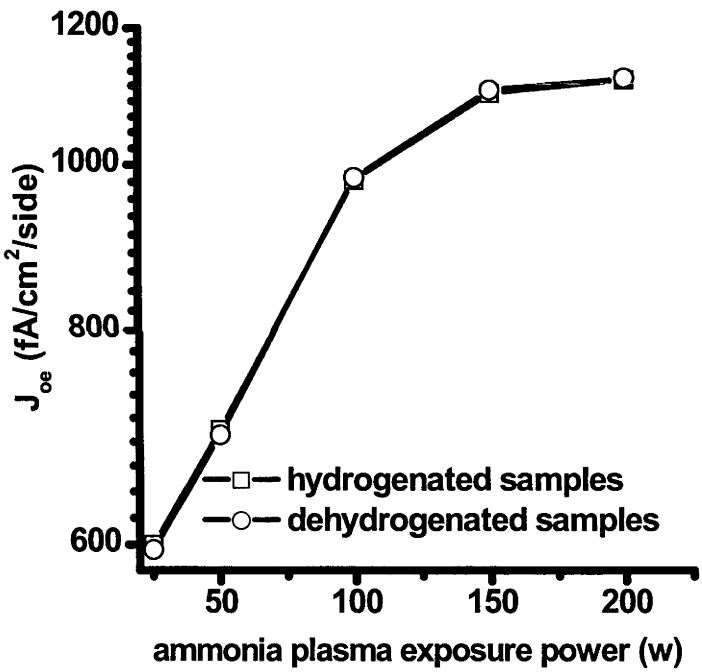

Figure 4.16. Power dependence of J_{oe} values after 5 minutes ammonia plasma exposure

4.3.4 Effect of post ammonia plasma exposure thermal annealing on interface properties

RTAs in dry nitrogen gas were carried out on samples just after ammonia plasma exposure at 200 W for 5 minutes. Both initially hydrogenated and de-hydrogenated samples were used for plasma treatments and subsequent thermal treatments, with nearly identical J_{oe} and C-V results.

Figure 4.17 shows the HFCV and QSCV curves for p type MOS stacks after ammonia plasma treatment at room temperature and an RTA at 400°C for 3 min in N_2, or FGA at 400°C for 30 minutes. For comparison, the corresponding curve for an as oxidized and forming gas annealed MOS stack is also shown.

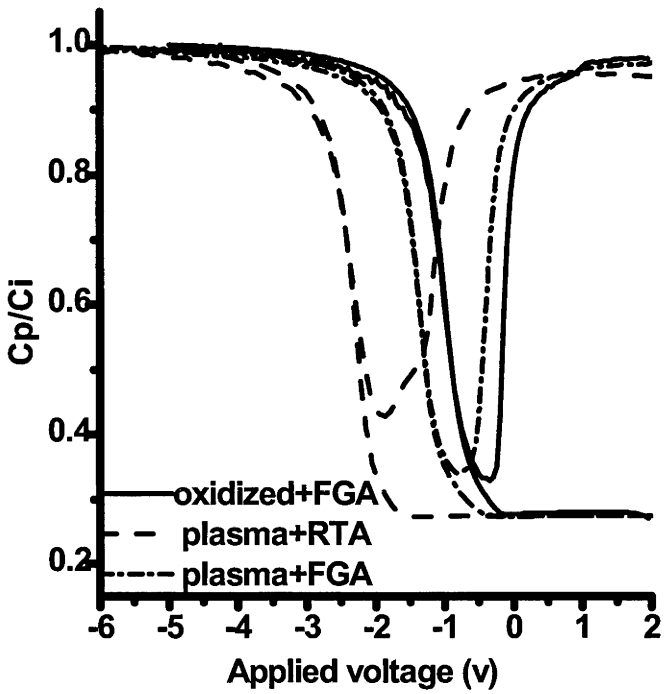

Figure 4.17. CV curves for p type MOS stacks prepared just after an oxidation and FGA; after oxidation, ammonia plasma and 400°C RTA; and after oxidation, ammonia plasma and FGA

It can be seen that the RTA treatment has resulted in C-V curves which are similar to the curves of the hydrogenated sample prior to the plasma treatment, indicating that many of the defects introduced by the plasma treatment have been removed. The FGA treatment results in a set of curves even more similar to the original, indicating a further reduction in (electrically active) defect concentration.

Figure 4.18 shows the J_{oe} values of plasma treated samples after 10 second RTAs in dry N_2 and after subsequent FGAs. Twelve samples were used, one for each RTA temperature (curve a) and subsequent FGA (curve b) at 400°C for 30 minutes. Figure 4.19 shows the defect density (D_{it}) at mid gap as a function of annealing temperature. Every anneal was carried out for 10 seconds.

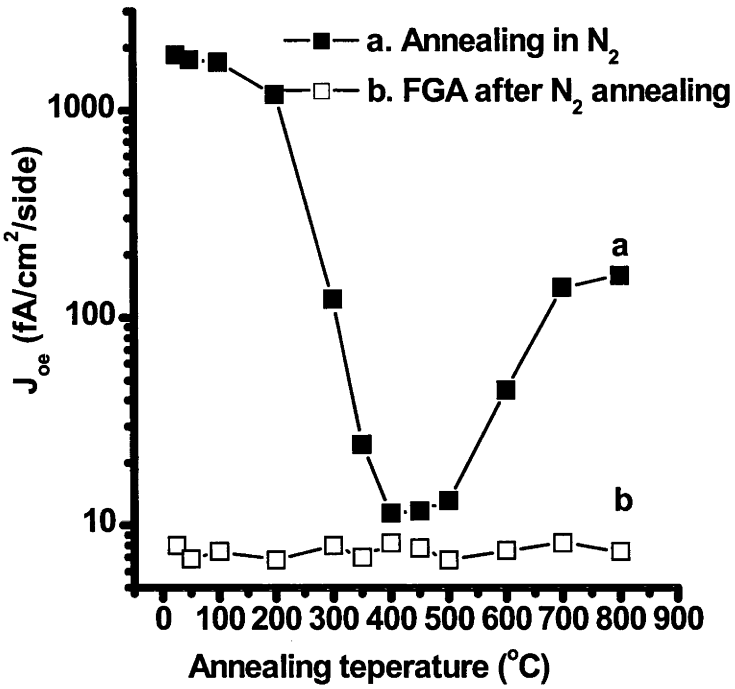

Figure 4.18. J_{oe} of plasma exposed samples after (a) RTA in N_2 for 10 seconds at temperature ranging from 25°C to 800°C, (b) subsequent FGA for 30 minutes after 10 seconds RTA.

The reduction in both J_{oe} and D_{it} following an RTA in the range 100-400°C is the result of the annealing of interface defects introduced by the plasma treatment. As the temperature is increased, a greater proportion of interface defects is annealed out. Above a temperature of ~450°C, both D_{it} and J_{oe} start to increase again as hydrogen atoms bonded to defects are gradually released. In other words, the increase in J_{oe} and D_{it} above 450°C is due not to the generation of additional defects, but to the activation of previously inactivated defects.

The FGA treatment following RTAs has the effect of both resulting in a further reduction in interface defect concentration (particularly for samples which had RTA treatments at temperatures below 400°C), and of re-hydrogenating the interface and thus rendering the majority of residual defects electrically inactive.

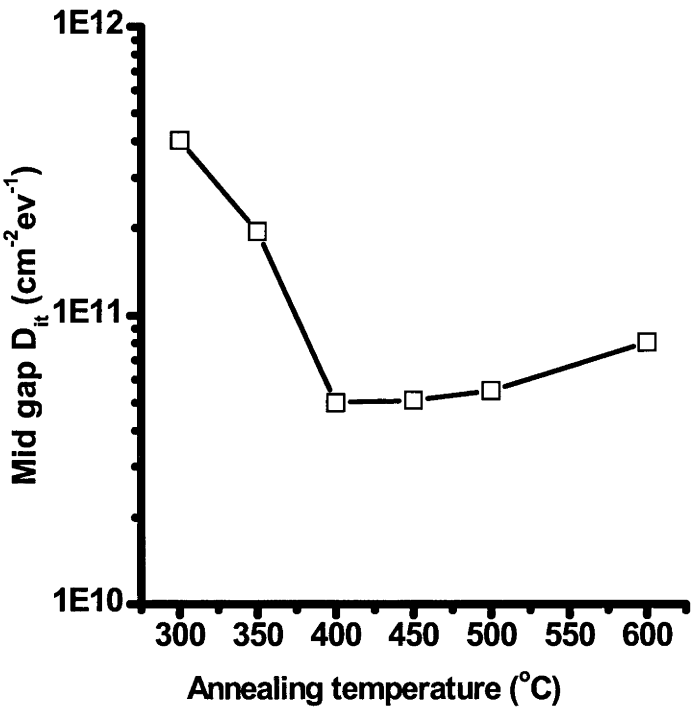

Figure 4.19. Mid gap D_{it} of MOS stacks prepared following plasma exposure and RTA in N_2 for 10 seconds at temperature ranging from 300°C to 600°C.

Figures 4.20 and 4.21 show the dependence of J_{oe} and mid gap D_{it} values on annealing time and temperature for RTAs in dry N_2. It can be seen that an anneal temperature of 400°C results in the lowest observed values for both J_{oe} and D_{it}. The fact that there is no further change for longer anneal times shows that no significant hydrogen release occurs at this temperature, consistent with previous experimental observations on oxidised, hydrogenated samples which had not been subjected to an ammonia plasma treatment. It is also apparent from figures 4.20 and 4.21 that at 400°C, the majority of the defects are annealed out rapidly (within the first 10 seconds).

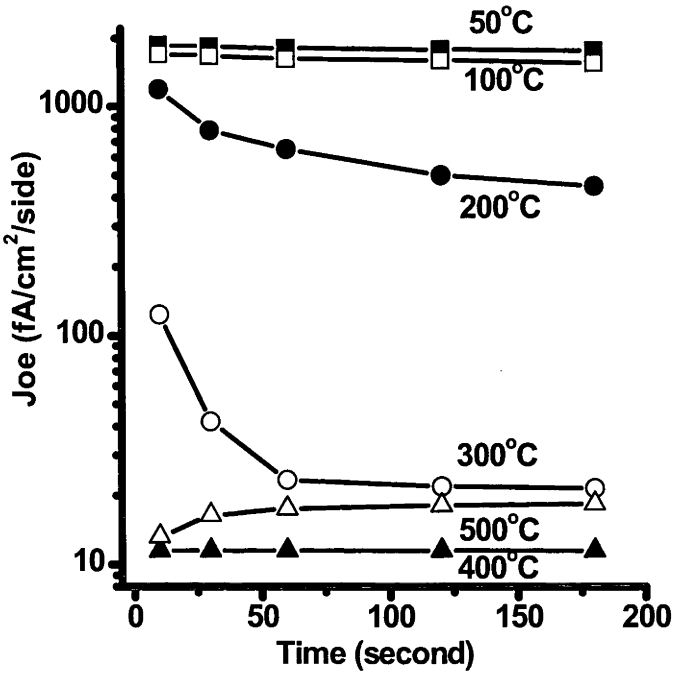

Figure 4.20. J_{oe} of samples following ammonia plasma exposure and subsequent RTA in N_2 for 10 to 180 seconds at temperatures ranging from 50°C to 500°C.

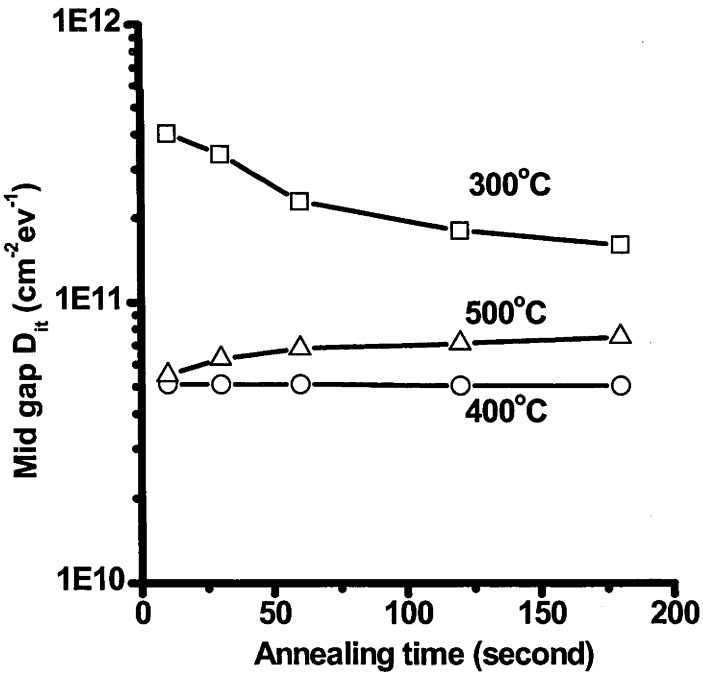

Figure 4.21 Mid gap D_{it} of MOS stacks following ammonia plasma exposure and subsequent RTA in N_2 for 10 to 180 seconds at temperatures ranging from 300°C to 500°C.

Table 4.2 summarises the values for mid gap D_{it}, charge density and J_{oe} for samples after various process steps. It is evident that an ammonia plasma treatment at 200 W for 5 minutes

and subsequent RTA at 400°C for 10 seconds is able to re-passivate initially de-passivated (de-hydrogenated) Si-SiO_2 interfaces. The diffusion of atomic hydrogen to the interface, generated by the dissociation of ammonia in the plasma, is believed to be responsible for the observed improvement. However, the same treatment results in a slight loss of passivation for an initially passivated (forming gas annealed) interface. The fact that an FGA following ammonia plasma results in a further improvement of the interface properties compared to an RTA indicates that the plasma treatment and RTA is not as effective at hydrogen passivation of defects as an FGA.

	As oxidized and hydrogenated	As oxidised and de-hydrogenated	Subsequent ammonia plasma	Subsequent ammonia plasma and RTA	Subsequent ammonia plasma and FGA
Mid gap defect density (10^{10} cm^{-2})	0.79	260	-	5.4	0.9
Positive charge density (10^{11} cm^{-2})	2.5	19	46	6.2	3.1
Emitter saturation current density J_{oe}(fA/cm^2/side)	6	160	1120	12	8

Table 4.2: Comparison of the mid gap defect density, charge density and emitter saturation current density following various processing steps. The RTA treatment was at 400°C for 10 seconds, the FGA was at 400°C for 30 minutes.

The results of table 4.2 also indicate that some of the interface defects introduced by the plasma treatment are not annealed out by subsequent RTAs. This can be seen by the slightly higher values for the midgap D_{it} following plasma treatment and FGA, compared to the initial, hydrogenated sample. The results are consistent with ammonia plasma exposure at 400°C.

Figure 4.22 displays the effective lifetimes as a function of injection level in the range 1×10^{15}/cm^2 to 1×10^{16}/cm^2. An oxide sample was FGAed (curve1) followed by ammonia plasma treatment (curve 2). RTA at 400°C for 3 minutes increases the effective lifetime dramatically (curve 3), while the following FGA further increases the lifetime (curve). RTA at 800°C for 3 minutes de-hydrogenate the samples (curve 5), however, the resulting lifetime is still much higher than the effective lifetime measured just after ammonia plasma exposure (curve 2). The results are in good agreement with the C-V and J_{oe} results.

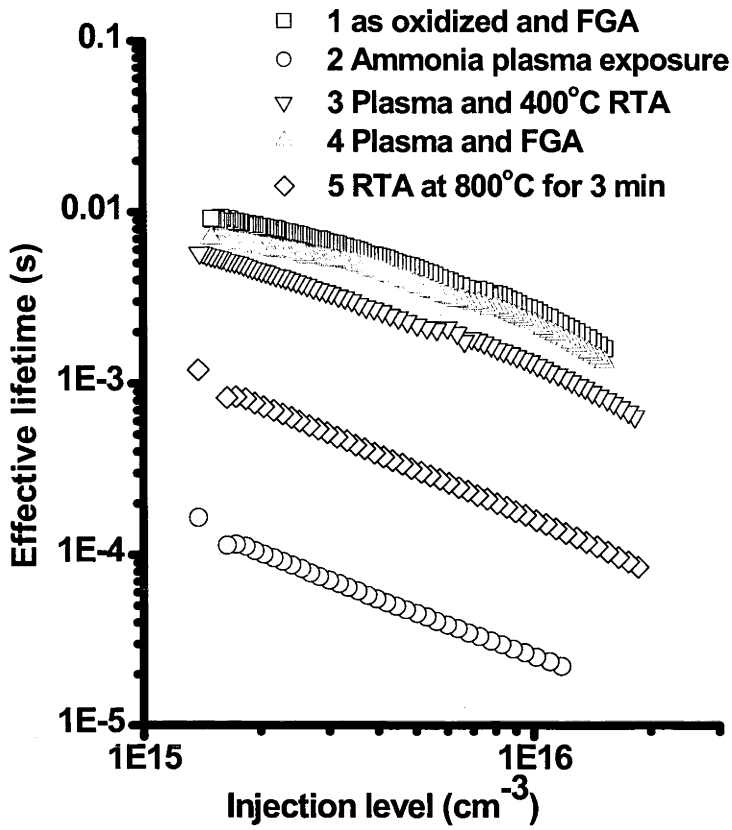

Figure 4.22. Effective lifetime for Si/SiO_2 stacks following various thermal steps.

4.3.5 Defect generation by room temperature ammonia plasma exposure – EPR results

EPR measurements were used to examine the properties of the paramagnetic interface defects on oxidised samples which had been exposed to ammonia plasma at 200 W for 5 minutes. Just after plasma exposure, no EPR signal could be detected, indicating that the majority of the additional defects generated by the plasma treatment are not paramagnetic, and that most of the paramagnetic defects are passivated by hydrogen. Samples were subsequently de-hydrogenated by RTA at 800°C for 3 minutes in N_2. As shown above, the RTA treatment also serves to remove the majority of the defects. For comparison, as-oxidised samples were given the same RTA treatment and measured by EPR. The results for the samples following RTA treatments are listed in table 4.3.

	g//	ΔB_{pp}// (G)	g⊥	ΔB_{pp}⊥ (G)	[Pb] (10^{12} cm-2)
No plasma treatment	2.00141	1.9	2.00860	3.8	4.6
With plasma treatment	2.00116	4.4	2.00866	5.3	7.8

Table 4.3. Comparison of the g value, peak to peak linewidth (ΔB_{pp}) and paramagnetic defect concentration of oxidized samples. Samples had received an RTA at 800°C for 3 minutes just before the measurements. '//' indicates magnetic field parallel to (111) direction, '⊥' indicates magnetic field perpendicular to (111) direction. The error in the g value is $4x10^{-5}$.

The EPR results clearly demonstrate that the ammonia plasma treatment has resulted in an increase in the density of paramagnetic defects which are not removed by thermal treatments at temperatures at or below 800°C. Another striking feature of the plasma treated samples is the decrease of g// and increase in the linewidth ΔB_{pp}// compared to the as-oxidised samples, both of which suggest a change of the Si-SiO_2 interface defect properties[129, 130].

4.3.6 Comparison of plasma NH_3 and plasma H_2 exposure of SiO_2/Si structures at room temperature

Figure 4.23 shows a comparison between plasma NH_3 and plasma H_2 exposure to SiO_2/Si structures. The atomic H source was described in section 4.2.4. After oxidation (1000°C in dry oxygen to give ~50 nm oxide) and an FGA, the J_{oe} value is around 5.5 fA/cm^2/side. 5 minutes plasma exposure dramatically increases the J_{oe} values (about 1100 fA/cm^2/side after ammonia plasma exposure and 600 fA/cm^2/side after plasma H_2 exposure). An RTA decreases the J_{oe} and the subsequent FGA further improves the Si-SiO_2 interface. For plasma H_2 exposure samples the J_{oe} after FGA returns to its 'as oxidized' level, but for plasma NH_3 exposed samples the J_{oe} is higher than the original level.

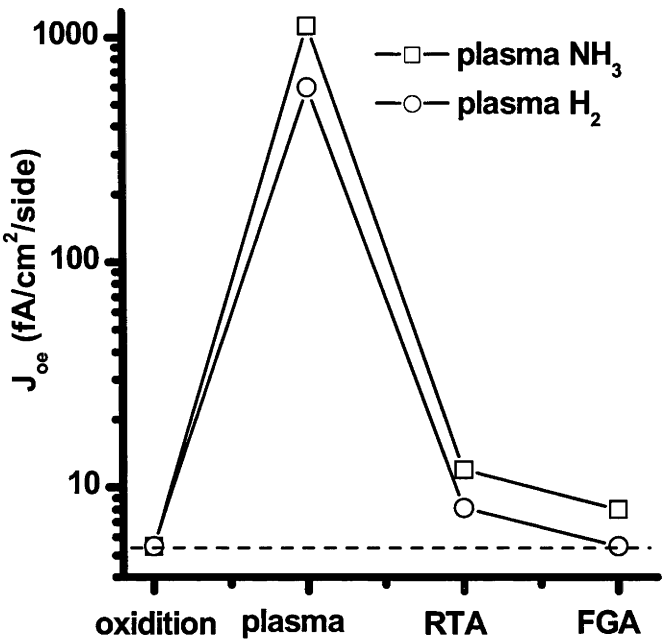

Figure 4.23. Emitter saturation current (J_{oe}) after various processing steps.

4.3.7 Influence of room temperature ammonia plasma exposure on thermal stability

Figures 4.24 and 4.25 and shows the J_{oe} values for SiO_2/Si structures following exposure to ammonia plasma as a function of RF power and exposure time. All samples received an RTA at 800°C for 3 minutes in nitrogen before lifetime measurements. At zero power, the sample received no plasma treatment. With an increase in plasma power from 25 W to 200 W, there is a substantial increase in J_{oe}, indicating that additional defects have been created which have not been removed by the RTA treatment. The result is in good agreement with the EPR measurements presented in table 4.3.

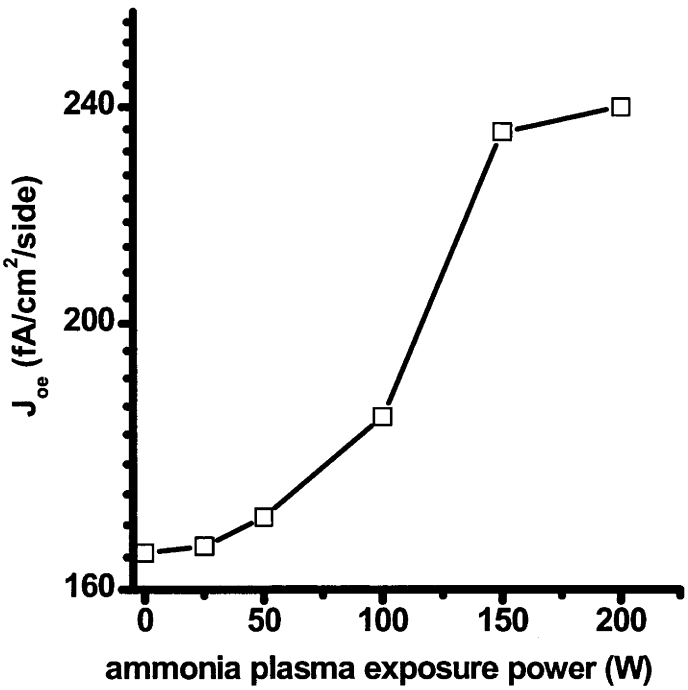

Figure 4.24. Power dependence of J_{oe} following 5 minute ammonia plasma exposure and subsequent RTA at 800°C for 3 minutes

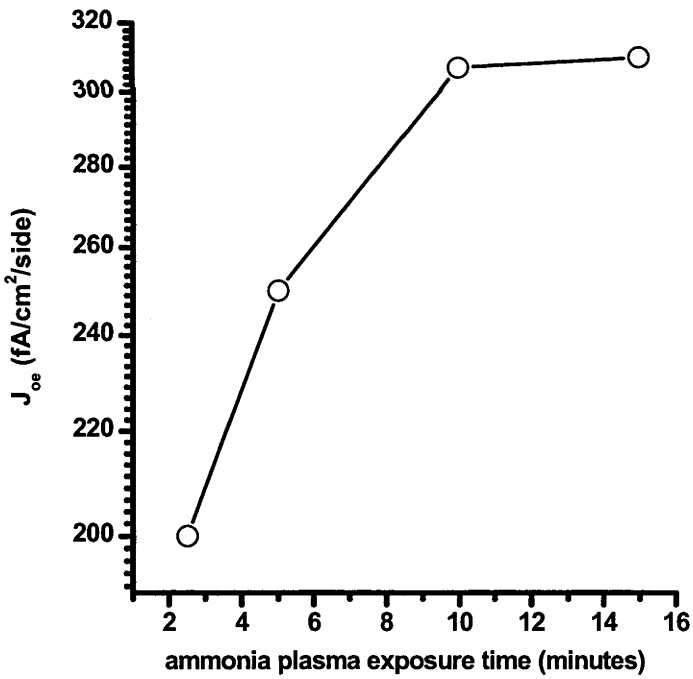

Figure 4.25. Time dependence of J_{oe} following ammonia plasma exposure at 200 W and subsequent RTA at 800°C for 3 minutes

4.4 Ammonia plasma exposure to $Si_3N_4/SiO_2/Si$ structures at 400°C

In the previous sections it was demonstrated that a hydrogen or ammonia plasma can introduce H rapidly to SiO_2/Si stacks and hydrogenate the $Si-SiO_2$ interface.

Hydrogen introduction into nitride films was discussed in Chapter 3 by annealing in forming gas at high temperature (800°C-900°C). However, the high thermal budget and long annealing time make this process of limited practical interest. In this section, we apply the ammonia plasma to nitride coated SiO_2/Si stacks.

4.4.1 Experimental methods

Float zoned, (100) high resistivity (≥ 100 Ω-cm), 500 μm thick as cut Si wafers were used for minority carrier lifetime measurements. After acid etching and RCA cleaning, both sides were passivated by a light phosphorus diffusion (with a sheet resistance R_{sh} of ~400 Ω/□ after thermal drive in) and a 50 nm thermal oxide grown at 1000°C followed by a 30 minute in-situ anneal in N_2 at the same temperature. Samples were annealed in forming gas at 400°C. 50 nm thick LPCVD Si_3N_4 films were deposited at 775°C, a pressure of 0.5 torr and ammonia to dichlorosilane (DCS) gas flow ratio of 4 to 1. The samples were subjected to a high temperature anneal (HTA) in N_2 at 900°C and 1000oC for 30 minutes to dissociate Si-H and N-H bonds in the nitride layer and de-passivate the $Si-SiO_2$ interface.

Samples were then exposed to ammonia plasma. An RF power of 200 W was used on samples at 400°C. Both sides of the samples were exposed to the plasma for equal amounts of time. This was followed by an anneal in N_2 at 500°C for 10 minutes for selected samples.

The effective lifetime (τ_{eff}) was measured by the QSS-PC method. The emitter saturation current density J_{oe} was determined from the slope of the inverse of τ_{eff} in high level injection.

Samples for Electron Paramagnetic Resonance (EPR) measurements were 25 mm×2.5 mm, p-type, ~10 Ω/cm, (111) Cz silicon wafers. A 50 nm thick oxide was grown and LPCVD deposition of 50 nm Si_3N_4 was done under exactly the same conditions as for the lifetime samples. Selected samples were exposed to the ammonia plasma under the same conditions as the QSS-PC samples (RF power of 200 W and a temperature of 400°C) for 10 minutes on each side. The nitride layer was removed from all samples by etching in hot phosphoric acid. Rapid thermal annealing was conducted at 800°C for 3 minutes to de-hydrogenate the $Si-SiO_2$ interface. The defect concentration was obtained by double integrating the signal and comparing with a standard solution signal taken under similar conditions.

Samples for MIR measurements are (111), double sided polished, ~500 μm thickness. The Si-H and N-H bond densities were measured. 200 nm thick Si_3N_4 films were deposited, under exactly the same conditions as for the QSS-PC samples, on both sides to achieve a good signal to noise ratio. These samples were also subjected to a HTA in N_2 at 900°C or 1000°C for 30 minutes, and subsequently exposed to ammonia plasma at 400°C.

Samples for SIMS measurements are (100), single side polished, ~500 μm thickness. Thermal grown 50 nm oxide was realized at 1000°C, without insitu N_2 annealing. 50 nm LPCVD Si_3N_4 was deposited at 775°C and 0.5 torr with ammonia to DCS ratio of 4:1. Before ammonia plasma exposure, those samples were annealed in N_2 at 400°C for 3 hours to balance the samples, since the annealing at 400°C was demonstrated to have little influence on H concentration in nitride layer. Subsequent ammonia plasma exposure was realized at 400°C for 20 minutes.

4.4.2 Hydrogen introduction into the LPCVD Si_3N_4 layer

4.4.2.1 Hydrogen introduction into the as deposited Si_3N_4 layer

The hydrogen concentration in LPCVD $Si_3N_4/SiO_2/Si$ stacks profiled by SIMS is shown in Figure 4.26. The SIMS date points show the hydrogen concentration (not deuterium). It can be seen that the ammonia plasma treatment has resulted in a substantial modification of the surface of the nitride layer and the creation of a region with a very high hydrogen concentration (region 1 in fig. 4.26), probably due to the effect of energetic hydrogen ions or hydrogen containing radicals. The diffusion of hydrogen through the nitride and oxide films is evidenced by the higher hydrogen concentration in region 2 of the nitride, the oxide, and the increase in the hydrogen peak at the $Si-SiO_2$ interface.

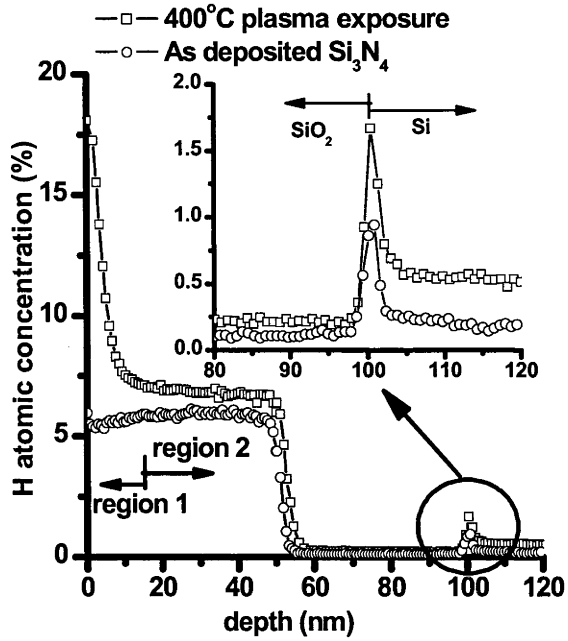

Figure 4.26. Hydrogen SIMS profile of the nitride layer, the SiO_2 layer and Si-SiO_2 interface of LPCVD $Si_3N_4/SiO_2/Si$ stacks before and after ammonia plasma exposure for 20 minutes at 400°C. Annealing in N_2 at 400°C for 3 hours was carried out just after nitride deposition.

4.4.2.2 Hydrogen introduction into annealed nitride layers

The IR absorbance spectra of some Si_3N_4 films are shown in figure 4.27. After annealing in N_2 at 900°C for 30 minutes, both N-H and Si-H bond densities decrease dramatically. Ammonia plasma exposure for 20 minutes on both sides of the sample re-introduces hydrogen into the nitride film and results in the re-formation of N-H and Si-H bonds. The concentration of N-H and Si-H bonds in the Si_3N_4 films following a HTA at 900°C or 1000°C for 30 minutes and ammonia plasma exposure at 200 W and 400°C is shown in figures 4.28 and 4.29.

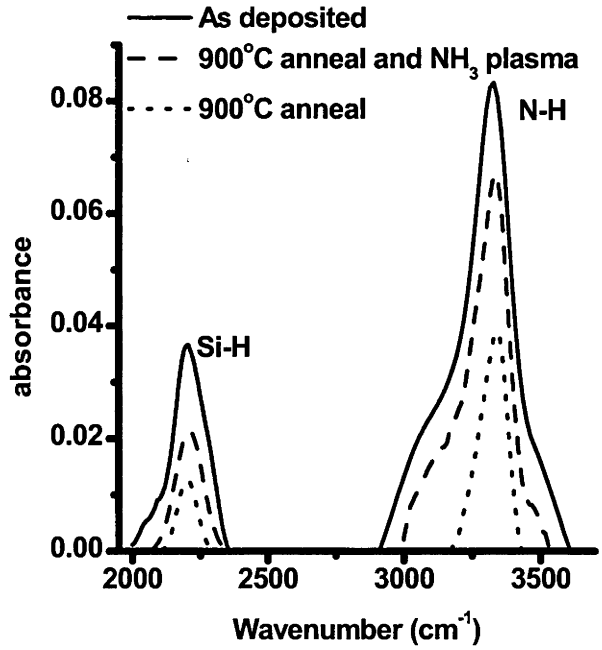

Figure 4.27. Absorbance spectra of the LPCVD nitride films showing N–H bonds (3331 cm^{-1}) and Si–H bonds (2202 cm^{-1}). The spectra are, in order from highest to lowest peaks: as deposited; 30 min N_2 anneal at 900°C and a subsequent ammonia plasma exposure for 20 minutes on both sample sides; and 30 min N_2 anneal at 900°C only

The N-H and Si-H bond concentration in the as deposited films is about 4.2% and 0.8% respectively, resulting in a total bonded H concentration of around 5.0%. After annealing in N_2 for 30 minutes, the total bonded H concentration drops to 1.1% and 0.6% for HTA temperatures of 900°C and 1000°C respectively, as shown in figures 4.28 and 4.29. The ammonia plasma re-introduces hydrogen and leads to a re-formation of Si-H and N-H bonds. The bonded hydrogen concentration saturates at around 3.7% and 1.9% for samples annealed at 900°C and 1000°C respectively, following a 40 minute ammonia plasma exposure.

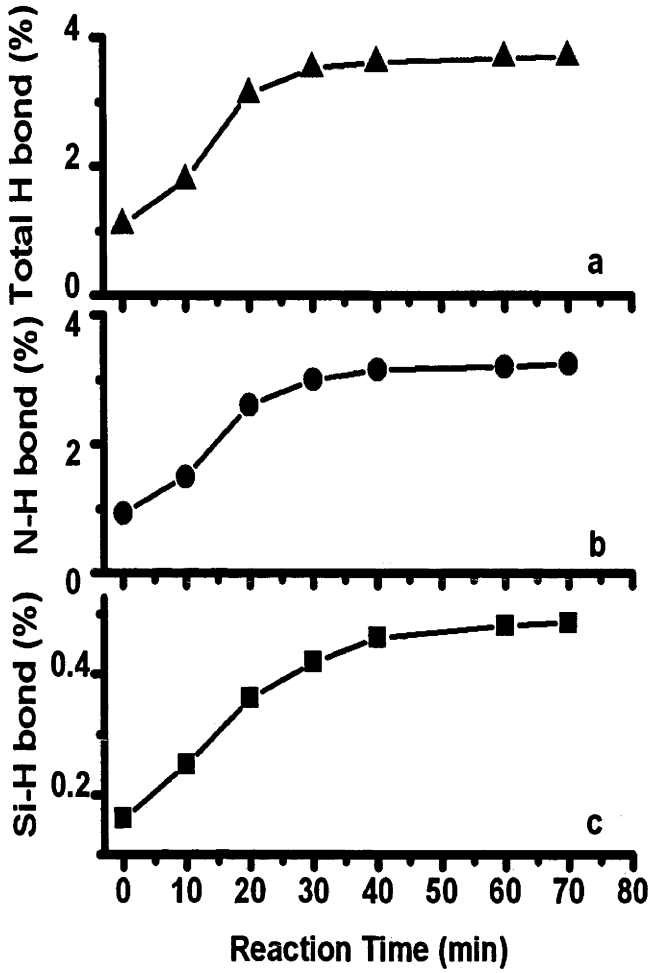

Figure 4.28. The Si-H, N-H and total (Si-H + N-H) hydrogen bond densities in LPCVD Si_3N_4 films following a 900°C N_2 anneal and subsequent ammonia plasma exposure, as a function of plasma exposure time

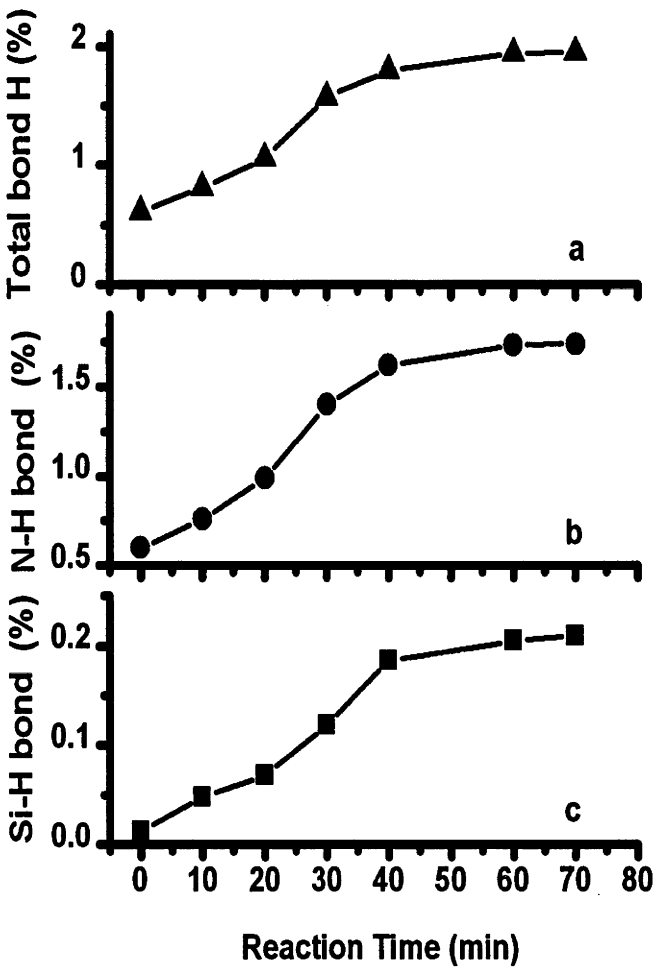

Figure 4.29. The Si-H, N-H and total (Si-H + N-H) hydrogen bond densities in LPCVD Si_3N_4 films following a 1000°C N_2 anneal and subsequent ammonia plasma exposure, as a function of plasma exposure time

It is worth noting that high temperature (840°C) anneals in forming gas (5% H_2 in 95% Ar) for several hours lead to very similar values for the saturated H bond densities, as shown in figure 3.8 and 3.9 in chapter 3, suggesting that this value is determined by the concentration of defects in the nitride film which are available for H passivation. (It should be noted, however, that the H concentration in fig. 3.8 and 3.9 may not yet have saturated after 4 hours, and that the saturated concentration for the high temperature forming gas annealed films may therefore be somewhat higher). The high temperature N_2 anneals result in a densification of the nitride film and a concomitant reduction in the concentration of available defect sites. The fact that the hydrogen re-introduction into the nitride film as reported here occurs more rapidly and at a lower temperature than when a forming gas anneal is performed, indicates that atomic hydrogen is diffusing directly into the film. In contrast, the diffusion of hydrogen using a forming gas anneal is speculated to proceed by the breaking of Si-H or N-H bonds formed in the surface region, in order to generate atomic hydrogen which then diffuses into the film[94].

4.4.3 Ammonia plasma passivation of the Si-SiO_2 interface of $Si_3N_4/SiO_2/Si$ stacks

Figure 4.30 shows the J_{oe} values for $Si_3N_4/SiO_2/Si$ stacks following an anneal in N_2 at 900°C for 30 minutes and a subsequent plasma ammonia exposure at 400°C with an RF power of 5 to 200 W for 5 minutes. The J_{oe} at zero power was measured just after annealing in N_2 (no plasma exposure).

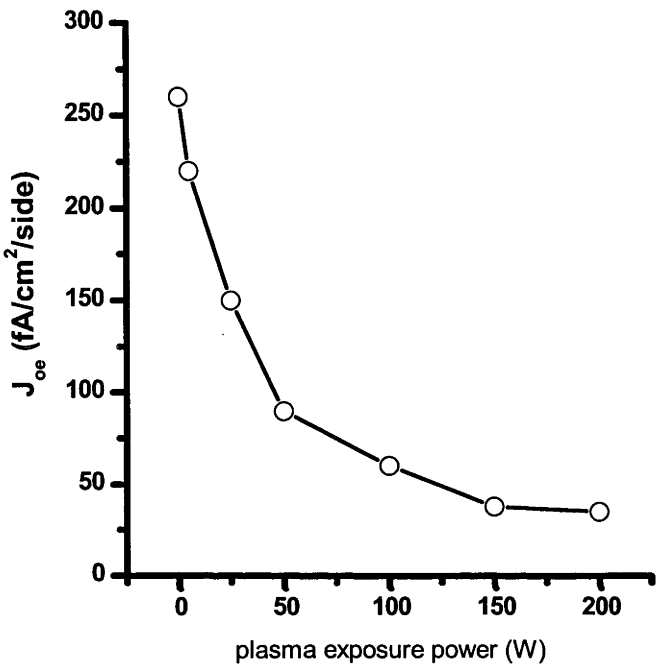

Figure 4.30 J_{oe} values with plasma exposure power for $Si_3N_4/SiO_2/Si$ stacks after plasma ammonia exposure at 400°C.

The value of J_{oe} increases following the HTA due to a loss of hydrogen from the Si-SiO_2 interface. The ammonia plasma exposure re-introduces H to Si-SiO_2 interface, causing J_{oe} to decrease. For a 5 minute exposure time, a higher plasma power results in better interface passivation. Figure 4.31 shows the J_{oe} values for $Si_3N_4/SiO_2/Si$ stacks after ammonia plasma exposure at 400°C and 200 W up to 20 minutes. The value of J_{oe} saturates after an exposure time of only 10 minutes. It should be noted that the nitride films used for the lifetime experiments are only 50 nm thick, in contrast to the 200 nm thick films used for MIR measurements. This explains the difference in the exposure time needed for saturation of J_{oe} (fig. 4.31) compared to the time required for saturation of H concentration (figs. 4.28 and 4.29).

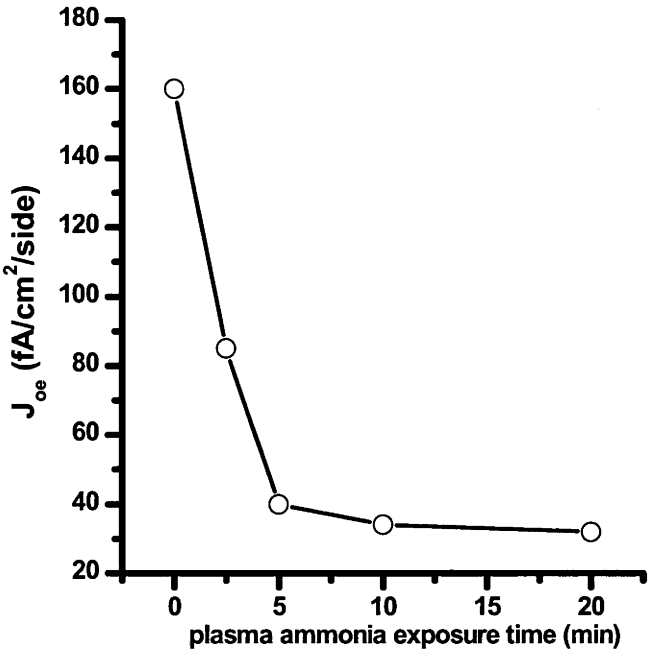

Figure 4.31 J_{oe} values with plasma exposure time for $Si_3N_4/SiO_2/Si$ stacks after plasma ammonia exposure at 400°C

4.4.4 Effect of thermal annealing after ammonia plasma exposure on Si-SiO_2 interface properties

Ammonia plasma exposure to $Si_3N_4/SiO_2/Si$ stacks re-introduces hydrogen to the Si-SiO_2 interface. After plasma exposure at 200 W for 5 minutes, samples were annealed in N_2 to study the influence of thermal treatments on the Si-SiO_2 interface. Figure 4.32 shows the dependence of J_{oe} on annealing temperature.

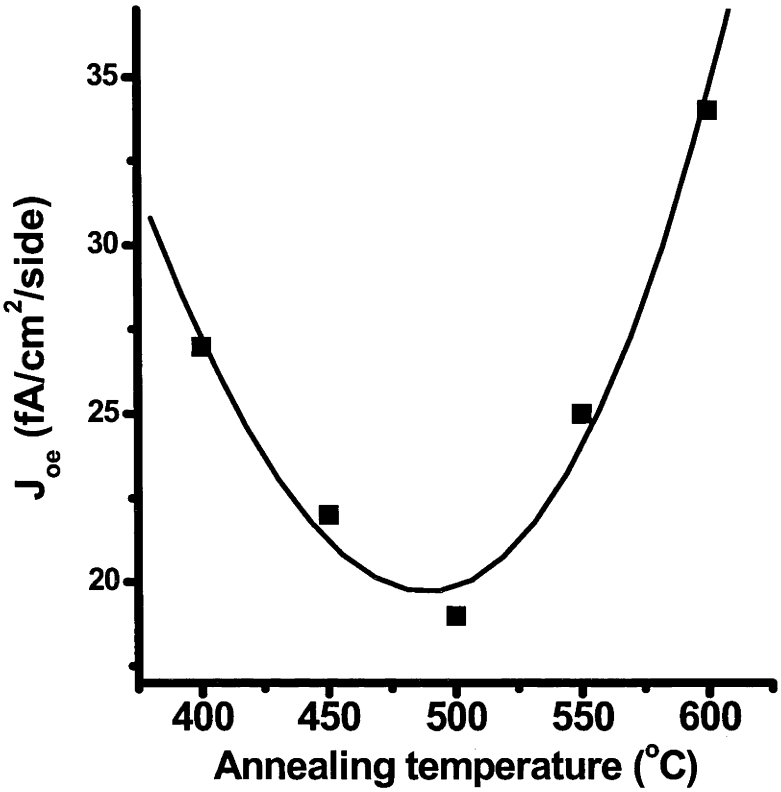

Figure 4.32 Temperature dependence of J_{oe} from $Si/SiO_2/Si_3N_4$ stacks for a 10 minute N_2 anneal following ammonia plasma treatment

Post ammonia plasma exposure anneals in N_2 further reduce the J_{oe} values. Even a 10 minute anneal in N_2 at 400°C results in an improvement in Si surface passivation. Figure 4.33 show the dependence of J_{oe} on annealing time. All samples received an ammonia plasma exposure at 200 W for 5 minutes just before annealing in N_2. It is concluded from these results that an anneal at 500°C for 10 minutes is optimal for the samples studied here.

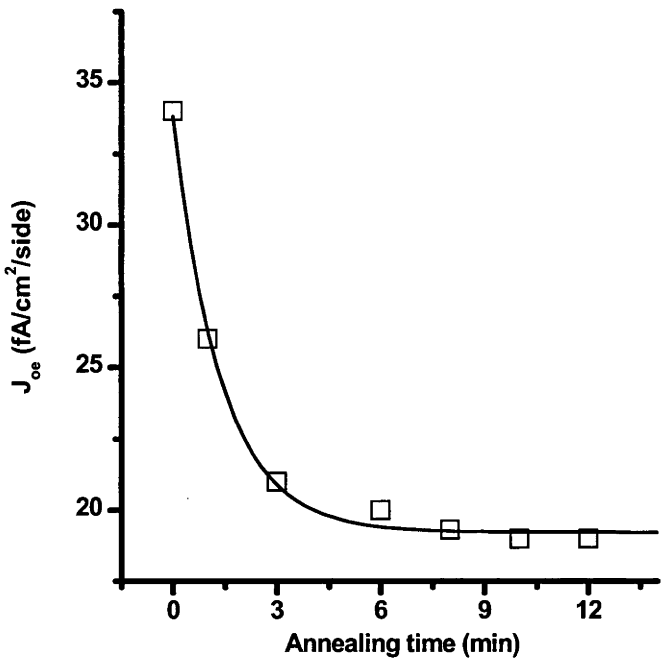

Figure 4.33. Time dependence of the emitter saturation current density J_{oe} of $Si/SiO_2/Si_3N_4$ stacks for a 500°C N_2 anneal following ammonia plasma treatment

The further improvement of surface passivation following anneals in N_2 at elevated temperatures is also evidenced by figures 4.34 and 4.35, which compare the J_{oe} values taken just after plasma exposure (as shown in figures 4.30 and 4.31) and after a subsequent anneal in N_2 at 500°C for 10 minutes.

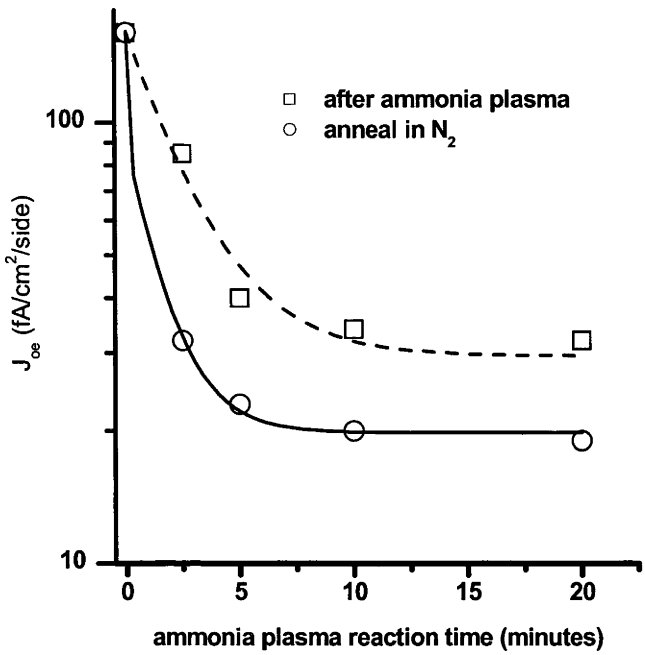

Figure 4.34. J_{oe} values for $Si/SiO_2/Si_3N_4$ stacks after HTA followed by (a) ammonia plasma exposure at 200 W for different times and (b) post ammonia plasma exposure annealing in N_2 at 500°C for 10 minutes.

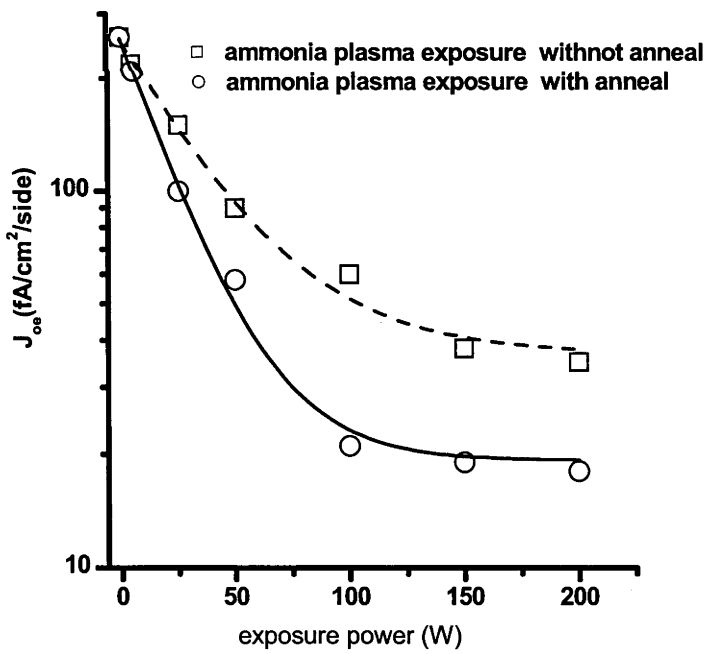

Figure 4.35. J_{oe} values for $Si/SiO_2/Si_3N_4$ stacks after HTA followed by ammonia plasma exposure at different RF powers for 10 minutes and post ammonia plasma exposure annealing in N_2 at 500°C for 10 minutes.

Ammonia plasma exposure to $Si_3N_4/SiO_2/Si$ structure does not introduce additional N atoms to the SiO_2 layer and interface, as shown in figure 4.36. The nitride and oxide are both 50 nm thick.

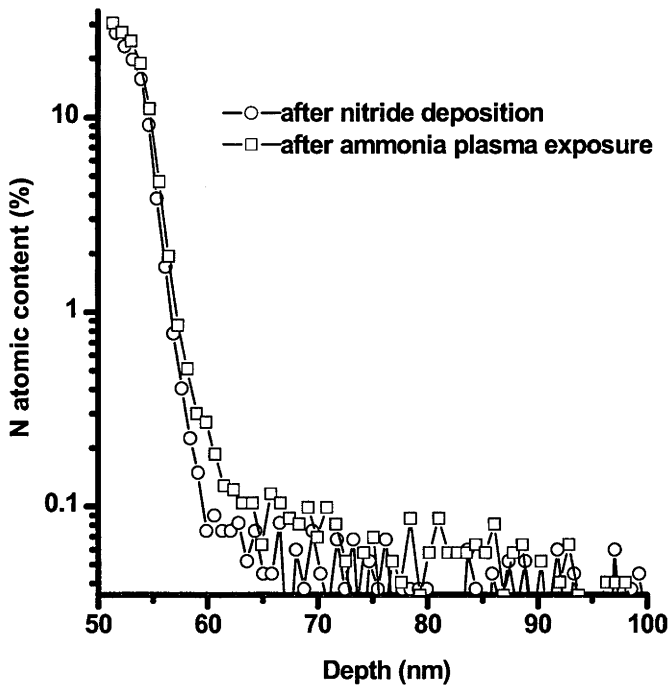

Figure 4.36. N SIMS profiles of the SiO_2 layer of $Si_3N_4/SiO_2/Si$ structures. No further nitridation is indicated by ammonia plasma exposure at SiO_2 layer and Si-SiO_2 interface. The nitride and oxide are both 50 nm thick.

The lowest J_{oe} value measured on samples following N_2 anneals after ammonia plasma exposure is 19 fA/cm^2/side, which is equal to the value of J_{oe} just after LPCVD Si_3N_4 deposition. The effective lifetimes of samples just after nitride deposition and after subsequent processing steps (HTA, ammonia plasma and N_2 anneal) are also similar at all measured injection levels, with a maximum value of about 5.1 ms. The high effective lifetimes and low J_{oe} values all indicate no significant degradation of the Si-SiO_2 interface or the Si bulk due to the ammonia plasma processing steps. In comparison, direct ammonia plasma exposure at 400°C on Si/SiO_2 stacks for 10 minutes increases the J_{oe} value to 85 fA/cm^2/side, much higher than the value for $Si_3N_4/SiO_2/Si$ stacks following plasma exposure. EPR measurements confirmed that samples with and without ammonia plasma treatments have the same paramagnetic defect concentration of 1.9×10^{13} /cm^2 after RTA dehydrogenation. When the magnetic field is set perpendicular to the (111) direction, angle dependent g values and peak to peak linewidth values are identical for both samples. This confirms that no further changes to the interface paramagnetic defect properties or density occurred as a result of the ammonia plasma treatment.

Although a post plasma exposure anneal in N_2 at 500°C can further improve the Si-SiO_2 interface properties, prolonged annealing at that temperature results in depassivation of the interface. The samples used in figure 4.34 were annealed in N_2 at 500°C for 2 days. The J_{oe} value increased from around 18 fA/cm^2/side to 30 fA/cm^2/side. This increase is likely to be due to a loss of hydrogen from Si-SiO_2 interface.

4.5 Ammonia plasma exposure to $Si_3N_4/SiO_2/Si$ structure at room temperature

In this section, ammonia plasma exposure to $Si_3N_4/SiO_2/Si$ structures at temperatures below 400°C is investigated. Room temperature (25°C) ammonia plasma exposure is discussed in detail.

4.5.1 Experimental methods

Samples for minority carrier lifetime measurements are FZ, (100) high resistivity (≥100 Ω-cm), 500 μm thick wafers. The wafers were etched by the producers before arriving at our lab. After acid etching and RCA cleaning, both sides were passivated by a light phosphorus diffusion (with a sheet resistance R_{sh} of ~400 Ω/□ after thermal drive in) and a 50 nm thermal oxide grown at 1000°C followed by a 30 minute in-situ anneal in N_2 at the same temperature. Samples were annealed in forming gas at 400°C. 50 nm thick LPCVD Si_3N_4 films were deposited at 775°C, a pressure of 0.5 torr and ammonia to dichlorosilane (DCS) gas flow ratio of 4 to 1. The samples were subjected to a high temperature anneal (HTA) in N_2 at 900°C for 30 minutes to dissociate Si-H and N-H bonds in the nitride layer and de-passivate the Si-SiO_2 interface.

Samples were then exposed to ammonia plasma in a plasma enhanced chemical vapor deposition (PECVD) reactor operating at 13.56 MHz. An RF power of 200 W was used on samples at 25°C to 400°C. Both sides of the samples were exposed to the plasma for equal amounts of time. This was followed by an anneal in N_2 at 500°C for 10 minutes for selected samples.

The effective lifetime (τ_{eff}) was measured by the QSS-PC method. The emitter saturation current density J_{oe} was determined from the slope of the inverse of τ_{eff} in high level injection.

Samples for SIMS measurements are (100), single side polished, ~500 μm thickness. A thermally grown 50 nm oxide was realized at 1000°C, without insitu N_2 annealing. 50 nm LPCVD Si_3N_4 was deposited at 775°C and 0.5 torr with ammonia to DCS ratio of 4:1. Before

ammonia plasma exposure, those samples were annealed in N_2 at 400°C for 3 hours. Subsequent ammonia plasma exposure was realized at 400°C for 20 minutes.

4.5.2 Effect of temperature of ammonia plasma exposure on Si surface properties of $Si_3N_4/SiO_2/Si$ stacks

Ammonia plasma exposure to $Si_3N_4/SiO_2/Si$ stacks was carried out at an RF power of 200 W for 5 minutes at temperature ranging from 25°C to 400°C. Before ammonia deposition, the $Si_3N_4/SiO_2/Si$ stacks were annealed at 900°C for 30 minutes in N_2. Figure 4.37 shows the J_{oe} values after ammonia plasma exposure at 200 W for 10 minutes and a subsequent annealing in N_2 at 500°C for 10 minutes.

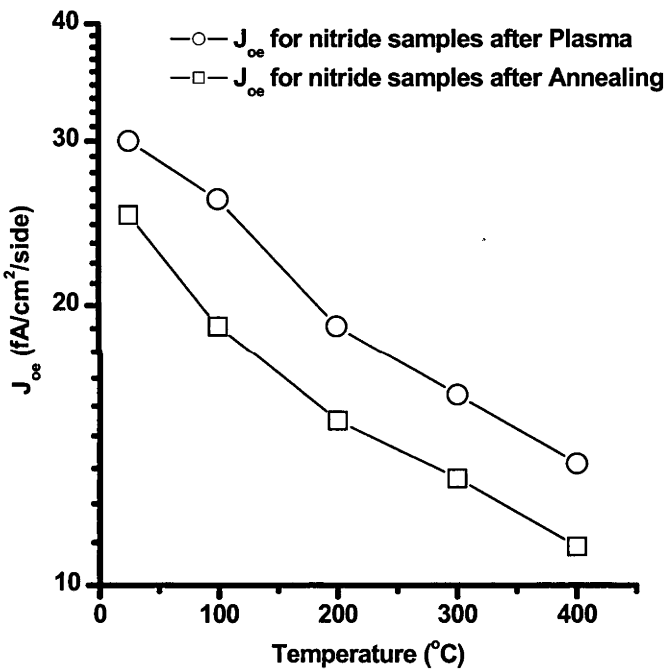

Figure 4.37 J_{oe} values for $Si/SiO_2/Si_3N_4$ stacks after HTA followed by ammonia plasma exposure at temperatures from 25°C to 400°C for 10 minutes and post ammonia plasma exposure annealing in N_2 at 500°C for 10 minutes.

In contrast to ammonia plasma exposure to SiO_2/Si structures at room temperature, no obvious increase of J_{oe} was detected. Room temperature ammonia plasma exposure and subsequent annealing in nitrogen at 500°C reduces the J_{oe} value. Plasma exposure at elevated temperature and subsequent anneals further reduce the J_{oe} values.

Figure 4.38 shows the H profile in $Si_3N_4/SiO_2/Si$ stacks. H profiles following plasma exposure at room temperature and at 400°C for 20 minutes are compared with an as deposited

stack. All the nitride coated samples were annealed in N_2 at 400°C for 2 hours after nitride deposition. No further processing was done on the samples prior to SIMS measurements.

Room temperature ammonia plasma exposure increases the H content in Si_3N_4 layer. In the nitride bulk, the H content is similar to that after 400°C ammonia plasma exposure. At the nitride surface, room temperature ammonia plasma exposure increases the H concentration, but still less than 400°C ammonia plasma exposure. Figure 4.38 also shows that atomic hydrogen from ammonia plasma exposure, even at room temperature, atomic H could be able to diffuse through nitride bulk. H content in oxide layer and Si-SiO_2 interface at $Si_3N_4/SiO_2/Si$ structures is shown in figure 4.38. Obvious hydrogen peak exists at Si-SiO_2 interface. Ammonia plasma exposure increases H content. Room temperature plasma exposure results in slightly higher interface hydrogen content.

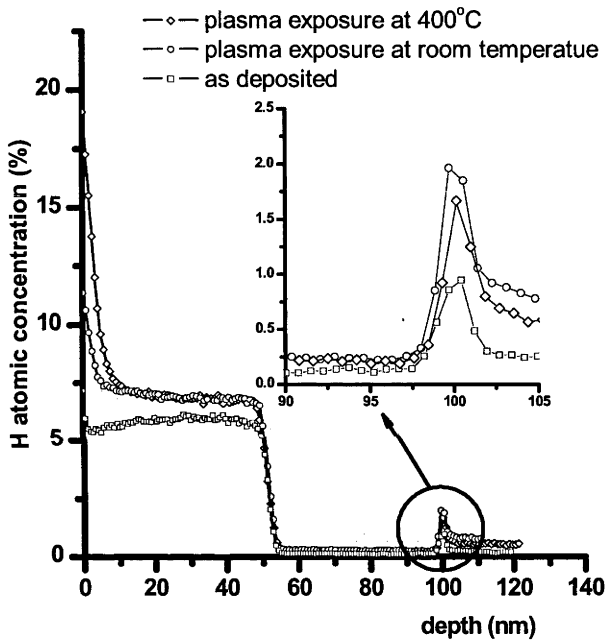

Figure 4.38. H profile in $Si_3N_4/SiO_2/Si$ stacks for as 'as deposited', and after ammonia plasma exposure at room temperature and 400°C.

However, Si surface passivation by room temperature exposure is inferior to the passivation realized by 400°C ammonia plasma exposure, for the exposure times used here. This may indicate a reduced flux of hydrogen to the Si-SiO_2 interface at lower temperatures, due to a lower diffusivity of the H in the dielectric films.

It is important to note that the J_{oe} measurements reported here were always on samples after an HTA at 900°C, in contrast to the SIMS samples, which did not receive a HTA. Comparison of the SIMS and J_{oe} results suggests that H diffusion in the annealed, densified nitride may be slower than in the un-annealed nitride.

4.5.3 Room temperature ammonia plasma exposure and subsequent annealing in nitrogen passivation on Si-SiO_2 interface at $Si_3N_4/SiO_2/Si$ stacks

Figure 4.39 shows the J_{oe} values for $Si_3N_4/SiO_2/Si$ structures after a high temperature anneal at 900°C for 30 minutes and ammonia plasma exposure at room temperature for 5 minutes at an RF power from 25 to 200 W and a subsequent anneal in N_2 at 500°C for 10 minutes. J_{oe} values at zero power come from the $Si_3N_4/SiO_2/Si$ structure after annealing in N_2 at 900°C for 30 minutes.

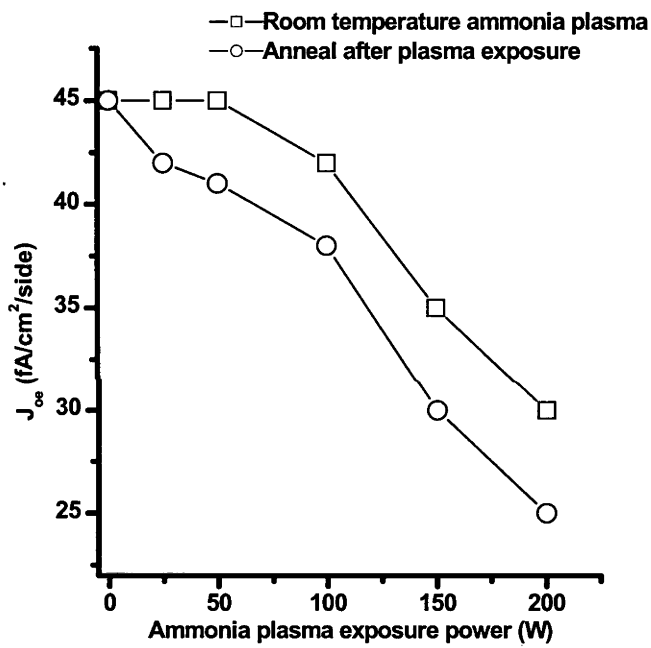

Figure 4.39. J_{oe} values for $Si/SiO_2/Si_3N_4$ stacks after HTA followed by ammonia plasma exposure at different power for 5 minutes and post ammonia plasma exposure annealing in N_2 at 500°C for 10 minutes.

At higher exposure powers, ammonia plasma exposure at room temperature results in better interface passivation. Subsequent anneals further improve the Si surface passivation. This result is in consistent with figure 4.35. Figure 4.40 shows the room temperature ammonia plasma exposure effect on $Si_3N_4/SiO_2/Si$ structures with reaction time. Room temperature ammonia plasma exposure occurred at 200 W. Longer reaction time and subsequent annealing in N_2 at 500°C for 30 minutes result in a better interface passivation.

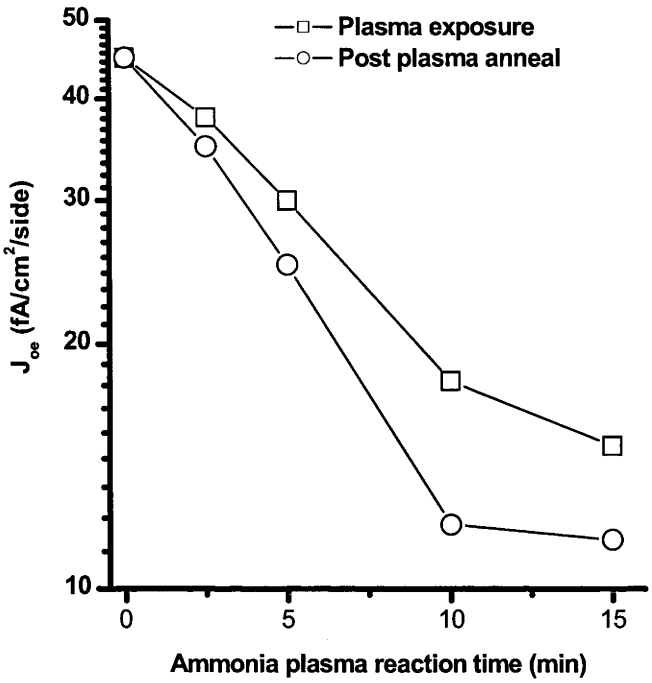

Figure 4.40. Joe values for $Si/SiO_2/Si_3N_4$ stacks after HTA followed by ammonia plasma exposure at 200 W for 2.5 to 15 minutes and post ammonia plasma exposure annealing in N_2 at 500°C for 10 minutes.

4.6 Discussion

In the section, the salient results presented in this chapter are discussed in detail

The increase in charge density following plasma NH_3 exposure has also been mentioned by other authors[128], indicating ammonia plasma causes radiation damage by breaking the Si-O bonds through the bulk SiO_2 film and forming the $Si-O_3$ and non-bridging oxygen centers, providing sites for positive charges. Fig 4.7 400oC ammonia plasma oxide

4.6.1 Plasma exposure of oxidised samples

4.6.1.1. Exposure to remote hydrogen plasma at room temperature

The results of section 4.3.6 show that room temperature atomic H from a remote plasma source introduces a wealth of damage at the $Si-SiO_2$ interface, as indicated by the dramatic increase in J_{oe} following plasma exposure. These defects can be annealed out. The results suggest that these

additional defects are completely removed by a short RTA at 400°C. The further improvement with a subsequent FGA is probably due to the re-passivation of defects (in particular P_b centres in the case of (111) surfaces, or P_{bo} and P_{b1} centres in the case of (100) surfaces) which were partly de-passivated by the atomic H treatment. Following an FGA the J_{oe} returns to its original level, suggesting no new defects have been introduced overall

These results are consistent with the results of Cartier et al[55]. Cartier carried out experiments where oxidised (111) oriented Si samples were subjected to a hydrogen plasma at room temperature. In these experiments, a remote plasma source was used, with H_2 as the source gas, and particular care was taken to prevent charged species from reaching the samples. Cartier et al. found, using EPR measurements, that such treatment resulted in significant passivation of P_b centres on an initially de-passivated Si-SiO2 interface, but slight de-passivation if the interface had initially been passivated using a forming gas anneal. In addition it was shown, using C-V measurements, that a high density of defects was generated by such a treatment, and that the majority of these defects were not paramagnetic.

Thus, the results presented here corroborate and expand on those of Cartier et al. In particular, the demonstration that the H induced defects can be removed with a short, low temperature anneal, is significant.

The nature of the defects, or the exact mechanism by which atomic H generates these defects, is not known at present. One possibility is that the defects are caused by radiation due to the recombination of atomic H to form H_2 in the vicinity of the sample, releasing 4.5eV photons. Radiation damage to oxidised silicon samples is generally observed to generate fixed positive charges in the proximity of the Si-SiO_2 interface, as well as additional Si interface states. The radiation damage can usually be annealed out at elevated temperatures in the range of 150°C to 500°C[131]. Dimitrova et al.[128] showed that radiation damage from ammonia plasma exposure could result in the dissociation of Si-O bonds throughout the bulk of the SiO_2 film and the formation of trivalent (Si-O_3) and non-bridging oxygen centers, both of which could behave as positive charge centers.

4.6.1.2 Exposure to remote hydrogen plasma at 400°C

The results of remote hydrogen plasma exposure of samples at 400oC (section 4.2.4) are similar to those at room temperature. Samples again show an improvement in J_{oe} following an FGA back to the value of the initial, passivated interface, indicating that no new defects were introduced and that the plasma treatment caused some de-passivation of initially passivated defects. Thus it appears that, even at the temperatures normally used for Si-SiO2 interface passivation using molecular hydrogen (typically 400oC, as was used throughout the thesis), passivation with atomic hydrogen is less efficient than molecular hydrogen.

It is interesting, in this context, to consider the effect of so-called alneals[16]. This treatment consists of evaporating a thin layer (~0.1 μm) of high purity (5N) aluminium onto the oxidised wafer surface, sintering the sample at 400°C in a forming gas ambient for 30 minutes and then etching off the aluminium using hot phosphoric acid (90°C). Alneals are well known to result in excellent surface passivation and alnealed surfaces have been measured to have a lower interface defect density D_{it} than forming gas annealed surfaces. The improvement afforded by such alneals has been supposed to be the result of the generation of atomic hydrogen due to the dissociation of water molecules at the SiO_2-Al interface. Our results would appear to contradict this hypothesis.

4.6.1.3 Exposure to ammonia plasma

Ammonia plasma exposure would be expected to result in the generation of the same type of defects that is generated by a remote H plasma. The results for room temperature ammonia plasma exposure in section 4.3 support this conclusion and indicate that these defects account for the majority of defects following plasma exposure. The finding that most of the defects generated at room temperature are not paramagnetic (section 4.3.5) is in agreement with the results of Cartier et al.[55]. In addition, the treatment results in the generation of a high density of positive charges, consistent with the hypothesis that radiation damage is the chief cause of defect generation.

The results of ammonia plasma exposure at both room temperature and elevated temperatures also indicate that the treatment results in some de-passivation of initially passivated defects (since in both cases there is an improvement following the FGA). Again, this can be ascribed to the action of the atomic H.

The fact that defect density does not return to the initial level of as oxidised and FGAed samples following a subsequent 400°C FGA (or in the case of EPR samples, an 800°C RTA) indicates that in addition, other defects have been generated at all process temperatures. In the case of the (111) samples used for EPR, at least some of these are additional, paramagnetic P_b centres. As well as generating additional P_b centres, the plasma treatment has resulted in a modification of the character of the P_b centres. Comparing the EPR results for room temperature and 400°C exposures, the change in the EPR 'signature' is almost identical for both cases. However, the defect density is larger for the 400°C exposure (~13×10^{12} vs 8×10^{12} for 5 mins at 200 W).

For the 400°C ammonia plasma samples it has been shown that the plasma treatment results in some interface and surface oxide nitridation, which is likely to be responsible for at least some of the observed increase in defect density, as well as the change in the EPR signature. In

fact, the observed changes in the EPR signature are very similar to those observed for nitrided oxides[119]. No SIMS measurements have so far been done on the room temperature ammonia samples, so it is unclear whether this treatment has caused nitridation as well. However, it might be expected that room temperature ammonia would lead to less nitridation given the requirement for the N containing species to be able to diffuse to the interface.

One explanation for the observed generation of additional defects is therefore that these defects may be exclusively the result of interface nitridation. If this hypothesis is correct then the extent of nitridation should decrease with decreasing plasma processing temperature, in line with the observed decrease in J_{oe} with decreasing temperature. Further, direct plasma exposure using H_2 as the source gas instead of ammonia should give similar results to the remote plasma exposure using H_2. These experiments are intended to be carried out at a future date.

4.6.2 Exposure of $Si_3N_4/SiO_2/Si$ stacks

The results of sections 4.4 and 4.5 show that atomic hydrogen is able to diffuse through the LPCVD Si_3N_4 layer and passivate the Si-SiO_2 interface, even at room temperature. In contrast to ammonia plasma exposure of samples with an oxide only, there is no evidence that additional, permanent defects are being generated when an LPCVD Si_3N_4 layer is present. This is consistent with the hypothesis that the additional permanent defects result from nitridation of the interface, since no additional nitridation is observed following plasma exposure with an oxide/nitride stack.

A further significant difference is that the dramatic increase in J_{oe} following room temperature plasma exposure, observed for samples with an oxide only, is not observed here. Thus, the nitride layer somehow prevents the generation of the responsible transient defects. It is possible that the presence of a nitride layer may shield the interface to a large extent from radiation damage, due to absorption of radiation within the nitride[132].

For ammonia plasma exposures at both room temperature and 400°C, a subsequent anneal is found to further improve interface properties. The fact that even an anneal at 400°C (the temperature of ammonia plasma exposure) results in some improvement in J_{oe}, whereas prolonged plasma exposure at the same temperature does not, suggests that this improvement is related to removal of defects generated by the atomic H itself. The optimal anneal parameters (temperature and time) correspond to conditions which minimise the loss of hydrogen bonded to interface defects while maximizing the removal of interface defects. However, the annealing dynamics are different from those observed for the defects generated by plasma exposure of samples with oxide only, since a higher anneal temperature and longer anneal time are required in order to minimise J_{oe}.

The temperature of the sample during ammonia plasma exposure does not appear to have a significant effect on the optimal degree of interface passivation that can be achieved, provided the ammonia plasma exposures are carried out for a sufficient period of time. The results show that longer exposure times are needed for lower sample temperatures, indicating a reduction in the H diffusion coefficient.

Finally, it should be noted that there is some discrepancy between some of the results. For example, the J_{oe} values following a 900°C N_2 anneal for 30 mins are not the same for all samples that received that treatment (compare e.g. fig 4.30 and 4.39 at zero plasma power). This is partly due to the fact that samples from different batches of wafers were used (for the former, wafers supplied as cut and for the latter, supplied acid etched. The surface treatment has been found to have a significant effect on the measured interface parameters, despite the fact that every effort was made to etch all wafers until a very high quality surface was obtained). There also appears to be some variability in the properties of the LPCVD nitride films over time, despite the fact that every effort was made to conduct all depositions using exactly the same deposition parameters. However, the observed discrepancies do not affect the observations made and the conclusions that have been drawn in this chapter since within each experiment and resulting data set, any variations between identically prepared wafers were small.

4.7 Summary

Ammonia plasma exposure of SiO_2/Si structures leads to the generation of additional defects, as well as to a slight de-passivation of existing interface defects, if these defects were initially well passivated by a forming gas anneal. If plasma exposure is carried out at room temperature, a high density of non-paramagnetic defects are formed, possibly as a result of radiation damage. In addition, a high positive charge density is observed. Subsequent anneals at 400oC completely remove these defects and reduce the positive charge density. In addition, ammonia plasma exposure leads to the generation of additional, paramagnetic defects, which cannot be removed by subsequent anneals at temperatures up to 800°C. These defects are likely to result from nitridation of the Si-SiO_2 interface.

Ammonia plasma exposure of Si_3N_4/SiO_2/Si structures leads to the diffusion of atomic hydrogen through the nitride film and to the Si-SiO_2 interface, even at room temperature, and allows the re-passivation of initially de-passivated (de-hydrogenated) Si-SiO_2 interfaces in such

structures. In contrast to SiO_2/Si structures, no dramatic generation of interface defects is observed for plasma exposure at room temperature, possibly due to the absorption of most of the damaging energetic radiation in the nitride layer. The presence of a nitride layer also prevents nitridation of the Si-SiO_2 interface.

Post plasma exposure anneals in N_2 are observed to further improve the interface properties, with optimal anneal parameters found to be 500°C for around 10 minutes. The improvement appears to be related to a removal of defects from the interface. However, further investigations would be required to obtain a clearer understanding of the reasons for the observed improvement.

Chapter 5

Conclusion and further work

5.1 Summary of the thesis

This work has experimentally examined the physical and chemical properties of LPCVD Si_3N_4 films, and the electronic properties of the Si-SiO_2 interface in SiO_2/Si and Si_3N_4/SiO_2/Si structures. Several characterisation techniques have been used for this work. The lifetime measurement techniques (the transient and generalised methods) are simple but powerful techniques that can quickly provide information on the Si surface recombination velocity with minimal additional sample processing. For lifetime-voltage measurements, an external voltage bias is applied to drive the Si surface from inversion to accumulation condition, allowing the the effective lifetime to be measured under the various surface conditions. This measurement

provides accurate information about the Si surface recombination velocity under inversion and accumulation conditions, we well as the Si bulk lifetime. The combination of high frequency and quasi static Capacitance-Voltage measurements allow quantification of the charge density in the insulator, the Si surface defect density and the defect distribution within the Si forbidden bandgap. EPR measurements enable the study of a specific defect, the Pb center, at the $Si-SiO_2$ interface. In particular, changes in the character and density of the (unpassivated) P_b centre can be determined, and correlated with changes in surface recombination. Thus, changes in $Si-SiO_2$ interface defect density (measured by C-V and EPR) and properties (from EPR), as well as changes in the insulator charge density (from flat band voltage measurements from high frequency C-V) can be linked to changes in the Si surface recombination velocity (from lifetime measurements).

An important factor affecting the Si surface and bulk properties is hydrogen. The bonded hydrogen spectra of Si_3N_4 films were observed using fourier transform infra-red spectroscopy (FTIR). Due to the low H concentration in LPCVD Si_3N_4 films, a variant of FTIR which has improved sensitivity, known as multiple internal reflection FTIR, was employed. In addition, on selected samples, the hydrogen profile in Si_3N_4 and SiO2 films was also measured using Second Ion Mass Spectroscopy (SIMS).

The SiO_2/Si interface is of fundamental importance in both the photovoltaic and microelectronic fields. The electronic properties at the $Si-SiO_2$ interface depend strongly on the oxidation conditions (temperature, oxidation ambient, and post oxidation treatments), as well as the Si surface orientation. The (111) orientation and textured surfaces display significantly worse thermal stability than the (100) orientation. In order to be able to study the interface in detail, it is of interest to be able to examine both well hydrogenated and completely de-hydrogenated interfaces. Hydrogenation was realized by annealing in forming gas and dehydrogenation could be realized by thermal annealing in a H free atmosphere.

Direct deposition of LPCVD Si_3N_4 film on Si causes irreversible Si bulk and surface damage. An oxide between Si and Si_3N_4 prevents this damage. However, deposition of a nitride changes the properties and density of $Si-SiO_2$ interface defects, concomitant with an increase of surface recombination velocity. The deposition condition greatly affects the $Si-SiO_2$ interface properties. The nitride coated structure displays a better thermal stability than the uncoated SiO_2/Si structure, due to the hydrogen in nitride film. Thermal annealing increases the density of the nitride film, shown by a lower etching rate in buffered HF solution. Thermal annealing was shown to cause irreversible damage to Si_3N_4/Si structures. For $Si_3N_4/SiO_2/Si$ structures, thermal annealing does not cause irreversible damage but leads to a loss of hydrogen from the interface for long, high temperature anneals. Forming gas annealing at high temperature introduces hydrogen back to nitride stacks after thermal processing.

The effect of plasma ammonia and plasma hydrogen gas exposure on the SiO_2/Si interface was studied and compared. At room temperature, radiation damage was found from both

sources. However, a low temperature thermal anneal was shown to be able to remove the radiation damage. Plasma exposure at 400°C does not result in radiation damage. Atomic H is able to passivate the dehydrogenated Si-SiO_2 interface, but results in slight depassivation of the hydrogenated Si-SiO_2 interface.

Plasma ammonia exposure to $Si_3N_4/SiO_2/Si$ stacks introduces hydrogen into nitride layer and re-passivates the dehydrogenated Si-SiO_2 interface at room temperature and at 400°C. The saturated hydrogen concentration depends on the thermal history of the nitride film. A post plasma exposure thermal anneal in nitrogen at 500°C for about 10 minutes further reduces the Si surface recombination velocity.

5.2 Suggested further work

5.2.1 Plasma Hydrogen exposure to nitride coated structures

Plasma ammonia exposure of nitride coated structures has been examined in this work. However, plasma hydrogen exposure also deserves in-depth research. Plasma hydrogen contains only neutral and charged hydrogen in atomic and molecular forms. A study of plasma hydrogen exposure of nitride coated structure could focus on the hydrogen concentration, bonding, the H profile in $Si_3N_4/SiO_2/Si$ structure, and the passivation of the Si-SiO_2 interface. The reaction temperature may range from room temperature to 400°C to study the H activity at different temperatures. The influence of post exposure anneals also needs to be examined.

The reason why a post plasma exposure anneal further reduces the Si surface recombination velocity is still not clear. One possibility is that the post plasma anneal drives atomic H from the nitride film into the Si surface and bonds with surface defects at 500°C. Plasma hydrogen exposure could be performed at elevated temperature (500°C) to check the Si surface properties after plasma exposure and post plasma anneal.

The influence of plasma hydrogen on the nitride film properties should also be studied. Plasma hydrogen could have the effect of reducing the charge density in the nitride film by bonding with defect sites. It is likely that plasma hydrogen exposure can reduce or eliminate the hysteresis effect caused by hole tunnelling at Si-Si_3N_4 interface.

5.2.2 Application of the Si_3N_4/SiO_2 double layer antireflection coating in solar cell

Excellent antireflection properties and good surface passivation can be achieved by Si_3N_4/SiO_2 double layer AR coats. Application of these structures to solar cells and examination of the solar cell parameters is of strong interest. A simple schematic structure is shown in figure 5.1.

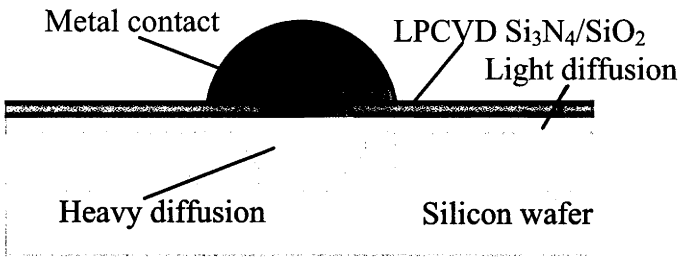

Figure 5.1: Illustration of the features of a typical LPCVD Si_3N_4/SiO_2 coated solar cell. The surface is usually textured; this is not shown.

A possible process sequence is as follows:

1 Texturing
2 Light phosphorus diffusion
3 Oxidation
4 LPCVD Si_3N_4 deposition
5 Open window for heavy diffusion and metal contact
6 Heavy phosphorus diffusion
7 Remove insulator from the back
8 Apply metal contact
9 Plasma H_2 or plasma NH_3 exposure the front side and anneal at 500°C.

The oxide (~25nm) and nitride (~50nm) thicknesses are optimized for good surface passivation and optical properties. The heavy phosphorus diffusion is carried out at a high temperature. The nitride layer is a good diffusion barrier. However, the high temperature processing results in a loss of hydrogen from the Si-SiO_2 interface. The plasma exposure re-introduces H and the anneal at 500°C optimises the surface passivation.

5.2.3 In-depth study of charge influence on Si surface properties

The charge density in SiO_2 and Si_3N_4 layers has been analysed in some detail in this work. Charge plays an important role in determining the degree of surface passivation, since interface recombination depends on the interface concentrations of electrons and holes, which are influenced by charge.

Charge introduction

The growth or deposition of dielectric layers (SiO2 and Si3N4 in this work) inherently results in charge in these films, due to the presence of charged defects, usually concentrated near the Si-dielectric or dielectric-dielectric interfaces. However, it would be of significant practical value if it was possible to deliberately control the density and distribution of charge in these layers.

The use of corona discharge allows the deposition of charge on dielectric surfaces in a simple, controllable and low cost way. However, this charge is usually not stable and is therefore only of use for characterisation purposes. The effect of corona charging on effective lifetime is shown in figure 5.2 for Si_3N_4/Si stacks. 50nm LPCVD nitride was deposited on a Si substrate.

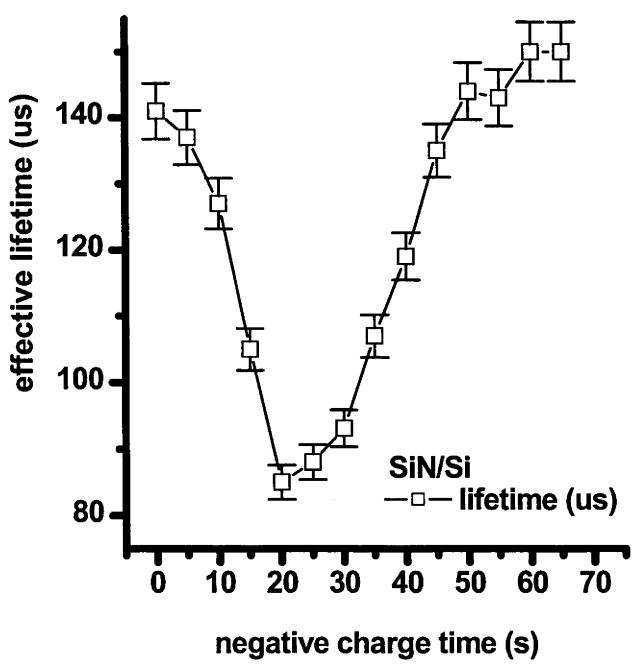

Figure 5.2. corona discharging effect on lifetime of Si_3N_4/Si structure

It can be seen that the effective lifetime is influenced strongly by the surface charge density.

Various attempts are reported in the literature to control and modify the dielectric insulator charge, chiefly by charging defects in the insulators. For example, some authors have diffused phosphorus and boron into SiO_2 layers. This has been found to result in moderate changes in charge density. This type of approach merits further investigation, using different dielectric layers.

Low temperature processes which may be able to add stable charges (positive or negative) to the insulator would be better still. It has been reported that, under certain circumstances (in particular, when a high potential difference exists across the insulator) corona charging can result in the creation of permanent, stable charge in the dielectric. This approach usually requires a pre-treatment of the dielectric for maximum effect. Further investigations into this approach appear warranted as well.

5.2.4 Use of LPCVD Si_3N_4 for n type solar cells

N type solar cells (feature an n type base) are attracting increasing attention because of their lower substrate cost. However, one important problem is that a boron diffused PECVD nitride-Si interface is difficult to passivate. It is generally believed that the passivation problem arises from the high density of positive charge in the PECVD nitride film that repel the majority carriers in p emitter. This should be tested and verified by lifetime-voltage measurements.

LPCVD Si_3N_4/SiO_2 stacks may be a good substitute to PECVD nitride for the passivation of the Si surface, due to the lower density of positive charge it contains. Boron diffusions are normally carried out at a higher temperature (~1000°C) than phosphorus diffusions. As was discussed in this work, phosphorus diffusions may introduce extra defects to the Si surface, demonstrated by the higher recombination velocity in accumulation and strong inversion region. The same problem may also exist for boron diffusions and this should also be checked by the lifetime-voltage method.

5.2.5 Comparison of the electronic and optical properties LPCVD and PECVD nitride films

A comparison between LPCVD nitride and the commercially widely used PECVD nitride films is desirable. LPCVD nitride is denser the PECVD nitride, so the commonly used metallization method (screen printing and firing) may not be suitable to LPCVD coated structures, or may

require significantly different firing parameters and/or paste composition. This could be investigated.

Another important issue is that PECVD nitride is a plasma-based deposition technology. Plasma technologies can introduce various problems (e.g. ion radiation damage) for Si surface passivation. The introduction of an SiO_2 layer between the PECVD nitride and the Si substrate may result in improved surface passivation and stability, by reducing the extent of such damage and by providing a very high quality interface. However, the introduction of an oxide layer may also require modification of firing parameters for the screen print paste.

5.2.6 UV stability

This work focused on the thermal stability of SiO_2/Si and Si_3N_4/SiO_2/Si structures. The UV stability of these and other structures is also of great practical interest. The results of studies on the UV stability of the Si-SiO_2 interface have been mixed [130-137], with some studies finding no degradation, while others indicate significant degradation under certain conditions. The UV stability can be influenced by many factors, including the exact UV spectrum and intensity, and the surface and interface properties (the type of dielectric material, surface doping, surface orientation, texturing and others). An in depth study of the UV radiation stability of diffused surfaces, such as are used in solar cells, could help to shed more light on this issue. In particular, it would be very beneficial to study changes in surface recombination, interface defect density and charge density on the same samples following UV exposure, in order to determine whether changes in surface recombination correlate with changes in interface charge, or interface defect density, or both.

List of Publications

Publications arising from the work in this thesis

Refereed Journal papers

[1] Hao Jin, K.J. Weber and A.W. Blakers, 'Hydrogen Passivation of LPCVD Si3N4/SiO2/Si Stacks by Ammonia Plasma Treatment', *Journal of The Electrochemical Society.* 154(6), H430-H434

[2] Hao Jin, K.J. Weber and P.J. Smith, 'Characterization of the Si-SiO2 interface following room temperature ammonia plasma exposure', *Journal of The Electrochemical Society.* 154(6), H417-H421

[3] Hao Jin and K.J. Weber, 'The Effect of Low Pressure Chemical Vapor Deposition of Silicon Nitride on the Electronic Interface Properties of Oxidised Silicon Wafers', *Progress in Photovoltaics: Research and Applications,* 15(5), 405, 2007

[4] Hao Jin and K.J. Weber, 'The effect of LPCVD silicon nitride deposition on the Si-SiO2 interface of oxidised silicon wafers' *Journal of The Electrochemical Society.* 154(1), H5-H8, 2007

[5] Hao Jin, K.J.Weber, W. Li and A. Blakers, 'Introduction of atomic H into Si3N4/SiO2/Si stacks', *Rare metals*, Vol 25, Special. issue, 150-152, 2006

[6] Hao Jin, K.J.Weber, A. Jayaprasad, P.J. Smith and A. Blakers, 'Si-SiO2 interface passivation by plasma NH3 and atomic H', *Rare metals*, Vol 25, Special. issue, 146-149, 2006

[7] Hao Jin, P.J. Smith and K.J. Weber, 'Introduction of Surface Defects on Oxidized Silicon by LPCVD Silicon Nitride Deposition', *Applied Physics Lettter*, 89(9), 092120-1 - 092120-3, 2006

[8] Hao Jin, K.J.Weber, P.N.K. Deenapanray and A.W.Blakers, 'Hydrogen Reintroduction by Forming Gas Annealing to LPCVD Silicon Nitride Coated Structures', Journal of The Electrochemical Society, 153(8), G750-G754, 2006

[9] Hao Jin, Klaus Weber , N.C. Dang , Wendy Jellett, 'Defect generation at the Si-SiO2 interface following corona charging' *Applied physics letter,* 90(26), 262109, 2007

Refereed Conference publications:

[10] Hao Jin, K.J. Weber, W. Jellett and A.W. Blakers, 'Influence of Phosphorous Diffusion on the Si Surface Passivation', *proceedings of 21th European Photovoltaic Solar Energy Conference, Italy, 3-7th, Sep, 2007*

[11] Hao Jin, K.J. Weber, W. Jellett and A.W. Blakers, 'Comparison of Plasma NH3 and Plasma H2 Exposure at Room Temperature on SiO2/Si and Si3N4/SiO2/Si Structures', *proceedings of 21th European Photovoltaic Solar Energy Conference, Italy, 3-7th, Sep, 2007*

[12] Hao Jin, K.J. Weber, P.J. Smith and A.W. Blakers, 'Defect Generation Concomitant with Plasma Nitridation to Si/SiO2 Stacks at Room Temperature', *proceedings of the 44th Annual Australian and New Zealand Solar Energy Society Conference, Canberra, Australia, 13-15, Sep, 2006*

[13] Hao Jin, K.J.Weber, and A.W.Blakers, 'Characterization of Low Pressure Chemical Vapour Deposited Si3N4 films', *proceedings of the 44th Annual Australian and New Zealand Solar Energy Society Conference, Canberra, Australia, 13-15, Sep, 2006*

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